High-Performance Embedded Systems-on-a-Chip

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Lecture 2: Birds-eye view (contd.)

Buzzwords

- Systolic Arrays
- Affine Control Loops
- Recurrence Equations
- Polyhedra
- Alpha
- Tiling

Source Programs: Affine Control Loops

- loop bounds:
  - affine expressions of surrounding loops;
  - or max/min of such expressions.
- loop body:
  - a loop;
  - an assignment statement;
  - a sequence of (any of) these two.
- Variables: index-vars or params , or (multidimensional) arrays
- Assignment statements:
  - lhs $\Longrightarrow$ array variable, accessed by affine function of indices;
  - rhs $\Longrightarrow$ expression containing such (indexed) array vars.

Example: Forward Substitution

```
S1:    x[1] := b[1]/a[1,1];
       for i = 2 to n do
S2:        s := 0;
           for j = 1 to i-1 do
S3:            s := s + x[j] * a[i, j];
           enddo
S4:        x[i] := (b[i] - s) / a[i,i]
          enddo
```

Recurrence Equations: Definition

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- $\mathcal{D} \subseteq \mathcal{Z}^n$ — domain of the equation.

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- *System of Recurrence Equations (SRE's):* set of (mutually recursive) equations. Could be uniform or affine (SURE or SARE).
- *Reductions:* associative/commutative operators applied to collections of data values

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  Alternatively:

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- Dual Representation: In terms of

- constraints: linear (in)equalities

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- or generators: vertices (& rays)

$$\{z \in \mathcal{Z}^n \mid z = a^T G;\ \sum_i a_i = 1\}$$

Change of Basis Transformation

Given an SRE

$$\begin{aligned} U[z] &= z \in D^u \; : \; g_u(\, U[f_{uu}(z)], \\ &\qquad\qquad V[f_{uv}(z)], \; \ldots \;) \\ V[z] &= z \in D^v \; : \; g_v(\, U[f_{vu}(z)], \\ &\qquad\qquad V[f_{vv}(z)], \; \ldots \;) \end{aligned}$$

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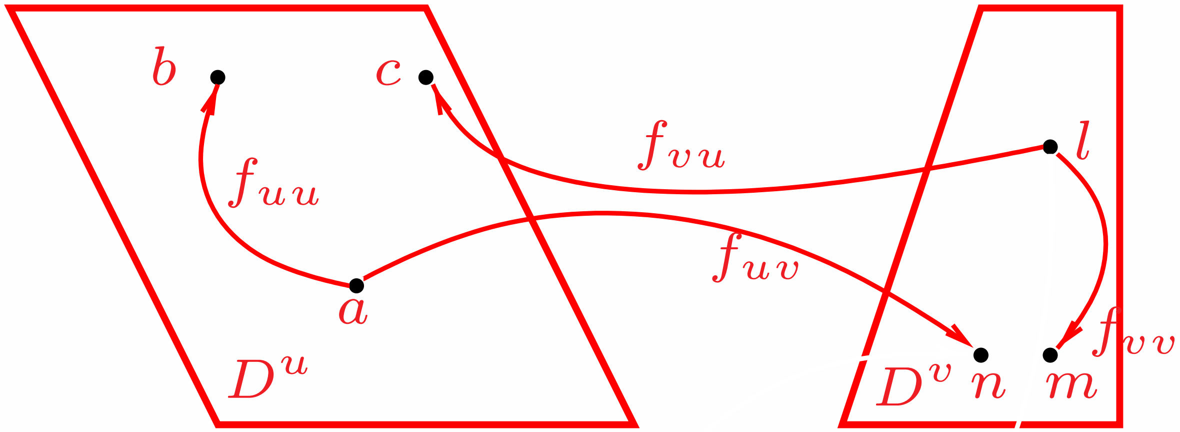
$$

and a function, $\mathcal{T}$, mapping original to new indices,

construct an equivalent SRE

Change of Basis



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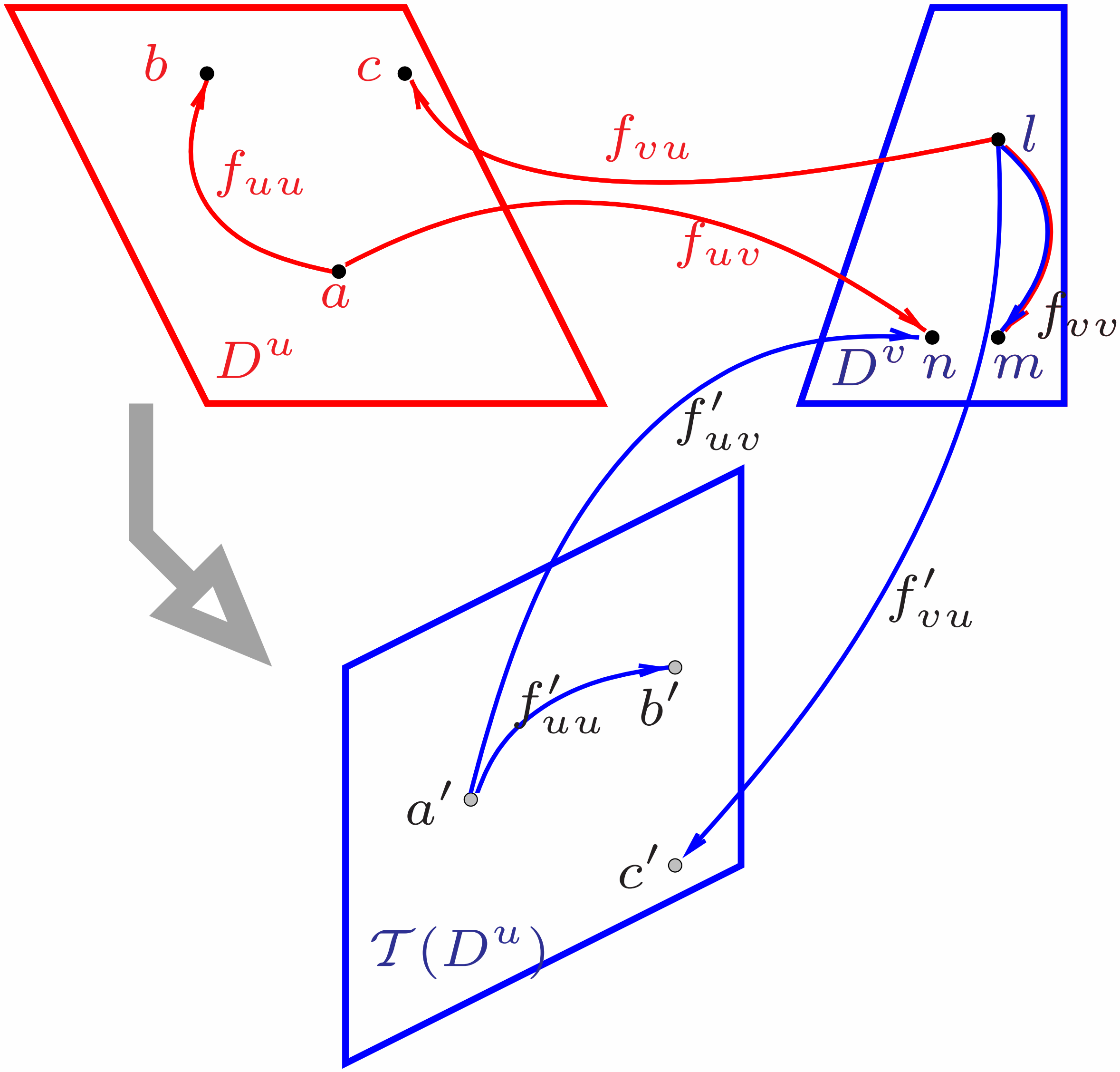

Transformed SRE

$$
\begin{aligned}
U[z] &= z \in \mathcal{T}(D^u) \;:\; g_u(\, U[\mathcal{T} \circ f_{uu} \circ \mathcal{T}'(z)], \\
&\qquad V[f_{uv} \circ \mathcal{T}'(z)],\ \ldots\ ) \\
V[z] &= z \in D^v \;:\; g_v(\, U[\mathcal{T} \circ f_{vu}(z)], \\
&\qquad V[f_{vv}(z)],\ \ldots\ )
\end{aligned}
$$

Closure Properties

Domains $\equiv$ Abstract Data Type (ADT), closed under:

- Intersection
- Union
- Preimage by the class of dependence functions
- Image by the class COB transformations

Also

- Transformations $\subseteq$ Dependence functions
- Dependence functions closed under composition

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Tiling/Partitioning/Loop Blocking

Partition the domains (iteration spaces of loops) into tiles (or blocks or supernodes)

Tiles are usually (hyper) parallelepiped shaped

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- power reduction in embedded systems.

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Optimally choose the tile parameters:

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Tile Sizing Problem: given the shape, determine the size to optimize a cost measure (running time)

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- Wolfe (1987), Irigoin & Triolet (1988), Schreiber & Dongarra (1990), Ramanujam & Sadayappan (1991) definitions and foundations

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- King, Chou & Ni (1990) — 2-D, square
- Hiranandani et. al (1994), Palermo et. al (1994) — 2-D one-pass

Our Results

- Andonov & Rajopadhye: (1994, 1996, 1997) multi-pass
- Andonov, et. al (1997, 1998) 3-d and n-D multi-pass
- Andonov, et. al (2000, 2001) 2-D oblique
- Derrien & Rajopadhye (2000) tiling for FPGA's
- Derrien & Rajopadhye (2001) tiling for power

Overview of the approach

- Build the tile graph
- Map to a p-processor parallel machine
- Determine running time with abstract parameters
  period, $\mathcal{P}$ and latency, $\mathcal{L}$
- Instantiate $\mathcal{P}$ and $\mathcal{L}$ with machine-specific model
- Solve discrete nonlinear optimization problem
- Experimental Validation