CS270 Worksheet – LC3 basics Name____

1) What does the PC register contain after the FETCH phase?
The memory address of the next sequential instruction.

2) Which phase happens first **EVALUATE ADDRESS** or EXECUTE?

3) Which phase happens first **DECODE** or FETCH OPERANDS?

4) What data types does the LC3 ISA support?
16 bit 2's complement integer

5) List the addressing modes supported by the operate instructions (ADD, AND, NOT)
Register, Immediate

6) Could an architecture be produced that had additional addressing modes for operate instructions? If yes what additional modes might be desirable?
Yes. Possible options are zero, one, or two registers being used by the operate instruction instead of three like in the LC3, also might want to be able to load operands directly from memory. Google ISA instruction formats for more info.

7) How can an OR instruction be simulated on the LC3?

```
OR R3, R1, R2    is equivalent to:    NOT R1, R1
                                      NOT R2, R2
                                      AND R3, R1, R2
                                      NOT R3, R3
```

8) What is this line of assemble code doing and why might it be necessary? AND R1, R1, #0
Initializing R1 to 0, this may be necessary because registers can contain any value before initialization

9) When would you use .BLKW? .FILL?
.BLKW N: allocate a block of memory with size N
.FILL N: allocate one memory location with value N

10) When would you use .STRINGZ? What is the last character produced by the assembler?
To create a null terminated array of characters in memory. The last character is '\0'

11) What is this instruction doing? STR R1, R2, #0
Storing the value in R1 at the location/memory address contained in R2

12) What instruction would you use to move a value in a memory location labeled Val to register R4.
LD R4 Val   This assumes that Val is within 256 addresses of the LD instruction.

13) Show two ways to set the value in the register R2 to 32.

```
Val    .FILL #32        or    AND R2, R2 #0
       LD R2, Val             ADD R2, R2, #8
                              ADD R2, R2, R2
                              ADD R2, R2, R2
```

14) What are the differences between the JMP and BR instructions
JMP is an unconditional branch so PC always is set to address found in source register.
BR is a conditional branch so if corresponding condition code is set the PC is set to address created from PC + offset.