

- 1) What does the PC register contain after the FETCH phase?
- 2) Which phase happens first EVALUATE ADDRESS or EXECUTE?
- 3) Which phase happens first DECODE or FETCH OPERANDS?
- 4) What data types does the LC3 ISA support?
- 5) List the addressing modes supported by the operate instructions
- 6) Could an architecture be produced that had additional addressing modes for operate instructions? If yes what additional modes might be desirable?
- 7) How can an OR instruction be simulated on the LC3?
- 8) What is this line of assemble code doing and why might it be necessary? `AND R1, R1, #0`
- 9) When would you use `.BLKW`? `.FILL`?
- 10) When would you use `.STRINGZ`? What is the last character produced by the assembler?
- 11) What is this instruction doing? `STR R1, R2, #0`
- 12) What instruction would you use to move a value in a memory location labeled Val to register R4.
- 13) Show two ways to set the value in the register R2 to 32.
- 14) What are the differences between the JMP and BR instructions