CS270 Cache Worksheet Name_____

1) Define the following terms

Cache:

Direct Mapped:

Tag:

Associativity:

Write back cache:

Write through cache:

Allocate on miss:

Compulsory miss:

Capacity miss:

Conflict miss:

Valid bit:

Dirty bit:

2) Given a 32 KB direct-mapped cache with a 64 byte block size, byte addressing, and 32 bit addresses, answer the following questions.

   a) Number of offset bits?

   b) Number of index bits?

   c) Number of tag bits?

   d) What index will the following address be mapped to 0xFA86A3D7 ?

   e) What tag will be associated with the above address?

   f) What extra bit of information will be needed if the cache is a write back cache?

   g) How many index bits will be needed if the cache is changed to a 2 way associative cache?

   h) How many index bits will be needed if the cache is changed to a fully associative cache?

   i) How many tag comparators will be needed if the cache is changed to an 8 way associative cache?