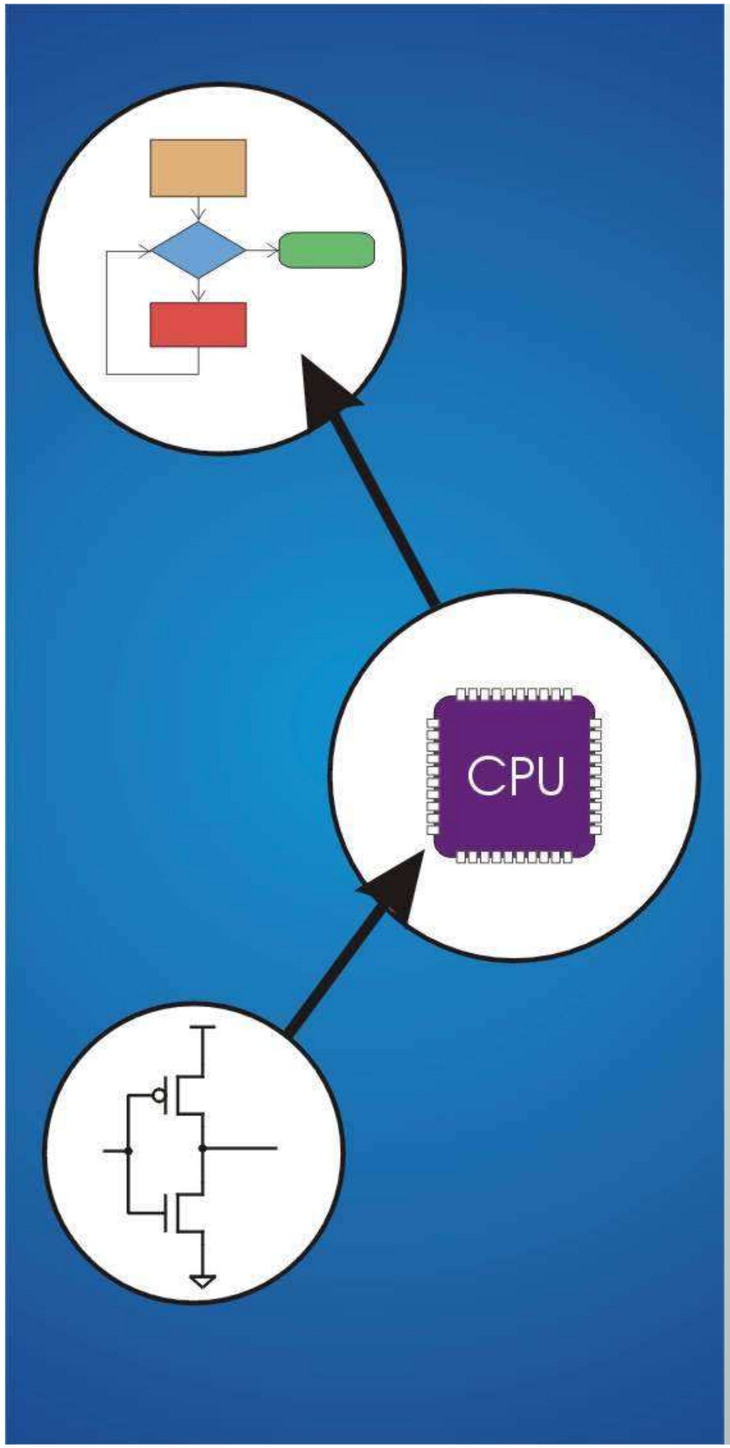
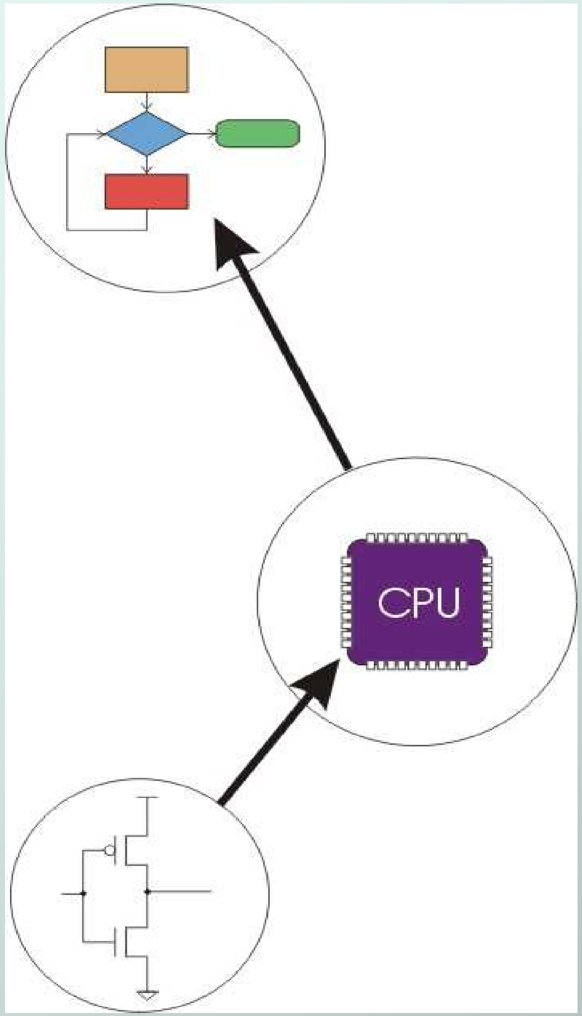


Chapter 3
Digital Logic Structures

Original slides from Gregory Byrd, North Carolina State University

Modified C. Wilcox, M. Strout, Y. Malaiya
Colorado State University

Computing Layers



Problems

Algorithms

Language

Instruction Set Architecture

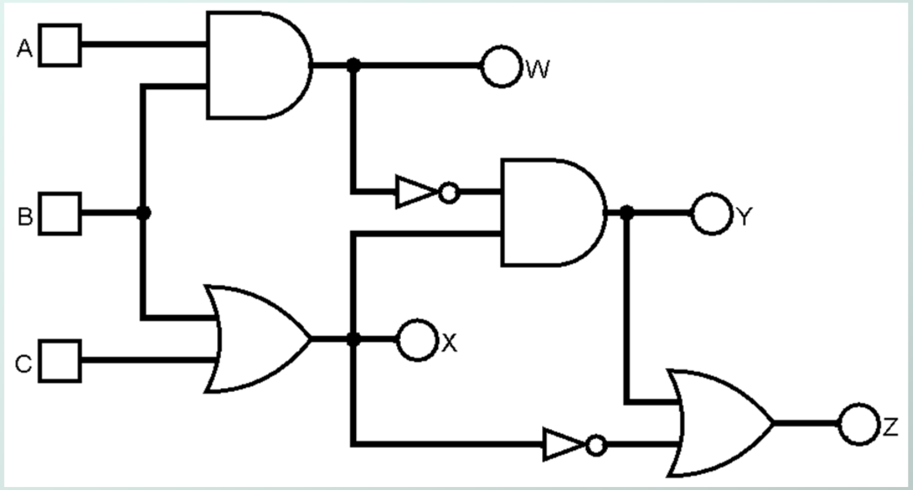
Microarchitecture

Circuits ←

Devices

Combinatorial Logic

- Cascading set of logic gates



A	B	C	W	X	Y	Z
0	0	0	0	0	0	1
0	0	1	0	1	1	1
0	1	0	0	1	1	1
0	1	1	0	1	1	1
1	0	0	0	0	0	1
1	0	1	0	1	1	1
1	1	0	1	1	0	0
1	1	1	1	1	0	0

Logic circuit and truth table

Logisim Simulator

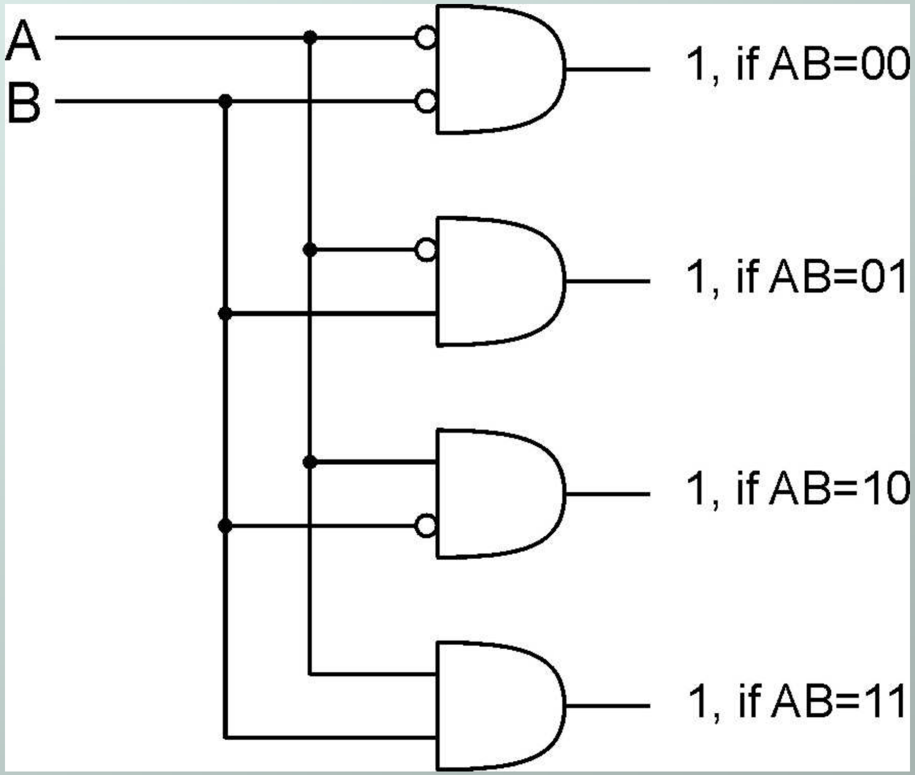
- Logic simulator: allows interactive design and layout of circuits with AND, OR, and NOT gates
- Simulator web page (linked on class web page)

  http://ozark.hendrix.edu/~burch/logisim
- Overview, tutorial, downloads, etc.
- Windows or Linux operating systems
- Logisim demonstration soon

n-to-2^n Decoder

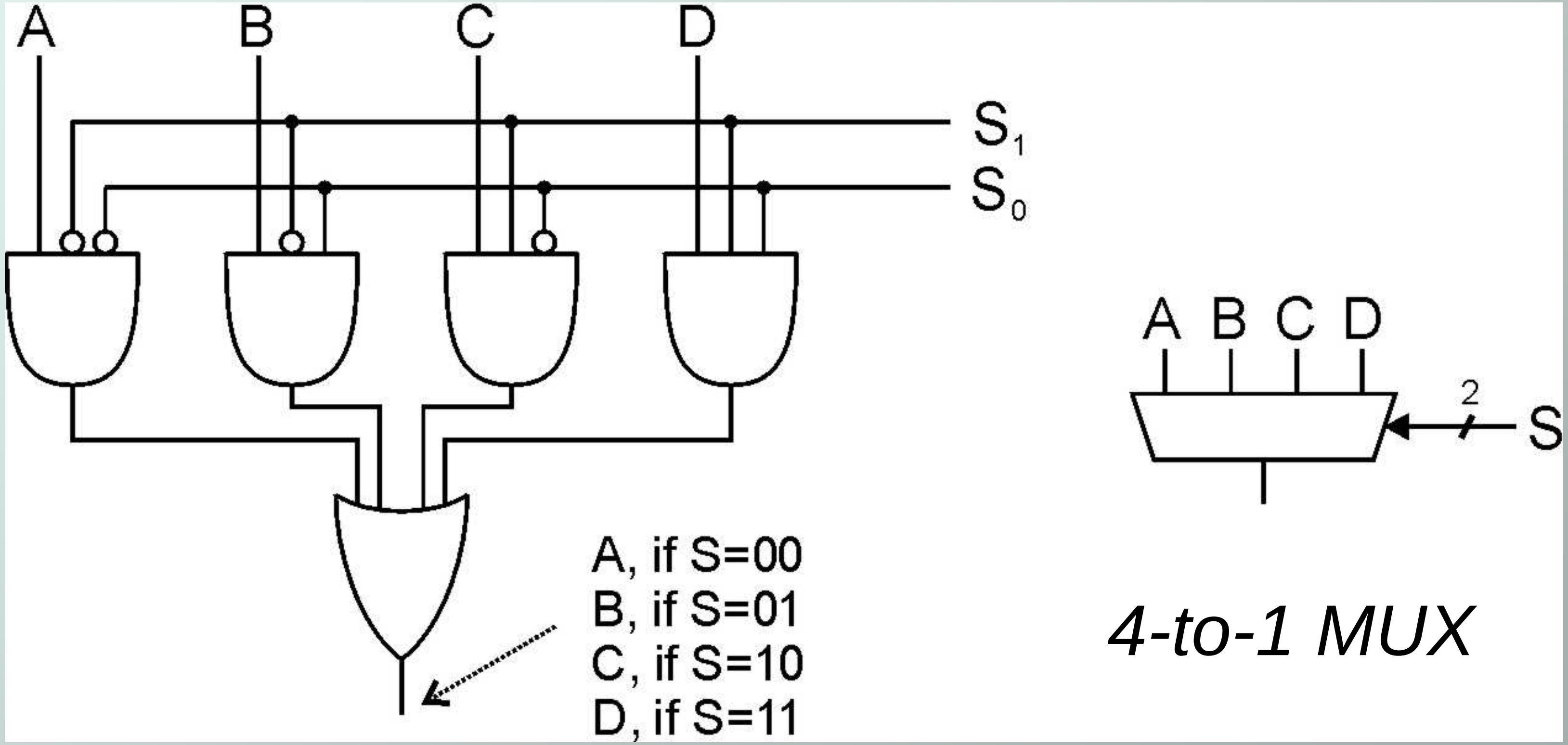
- *n* inputs, *2^n* outputs
  - exactly one output is 1 for each possible input pattern

2-to-4bit decoder



Multiplexer (MUX)

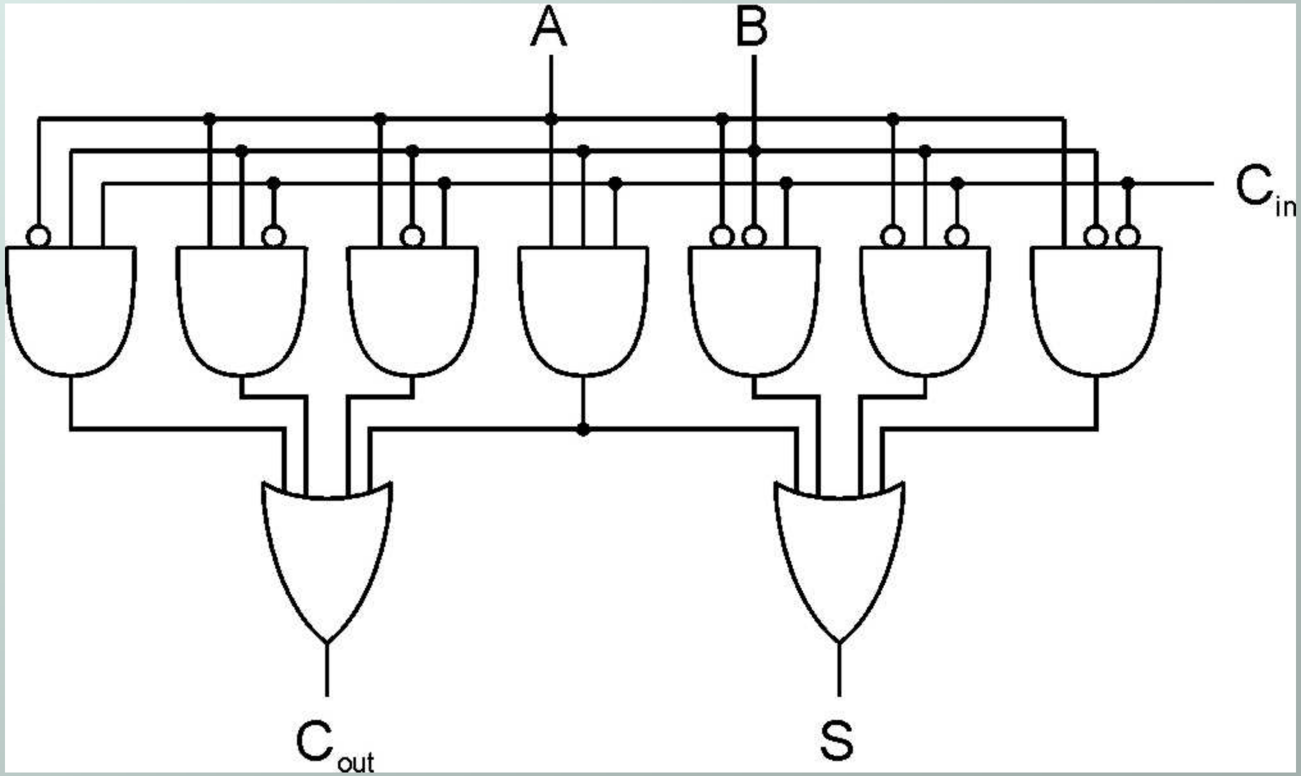
- *n*-bit selector and *2*^{n} inputs, one output
  - output equals one of the inputs, depending on selector



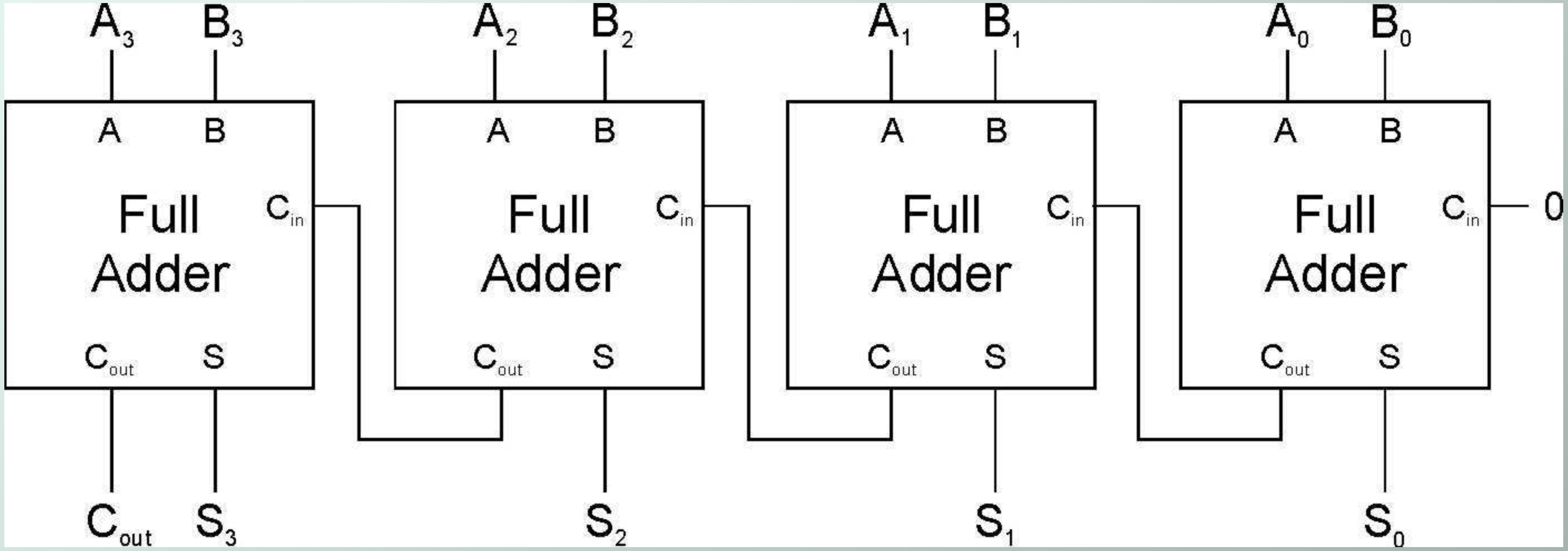
Full Adder

- Add two bits and carry-in, produce one-bit sum and carry-out.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



Four-bit Adder



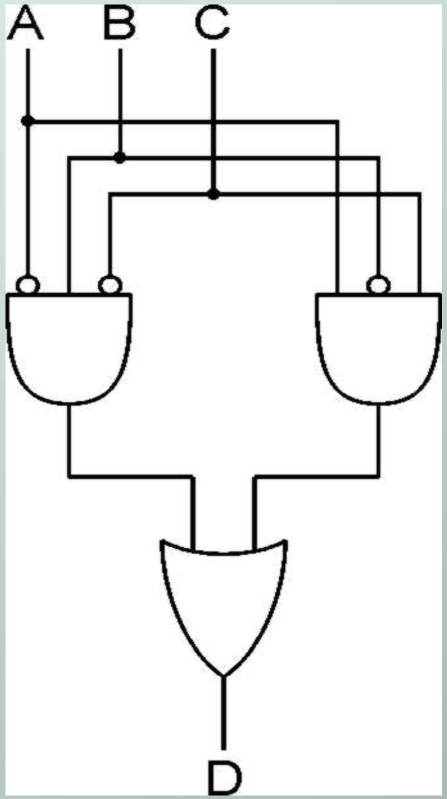
Logisim Demos

- Let us look at some of these using Logisim simulation.

Logical Completeness

- Can implement <u>ANY</u> truth table with combo of AND, OR, NOT gates.

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0



1. AND combinations that yield a "1" in the truth table.
2. OR the results of the AND gates.

“two-level” “AND-OR” implementation

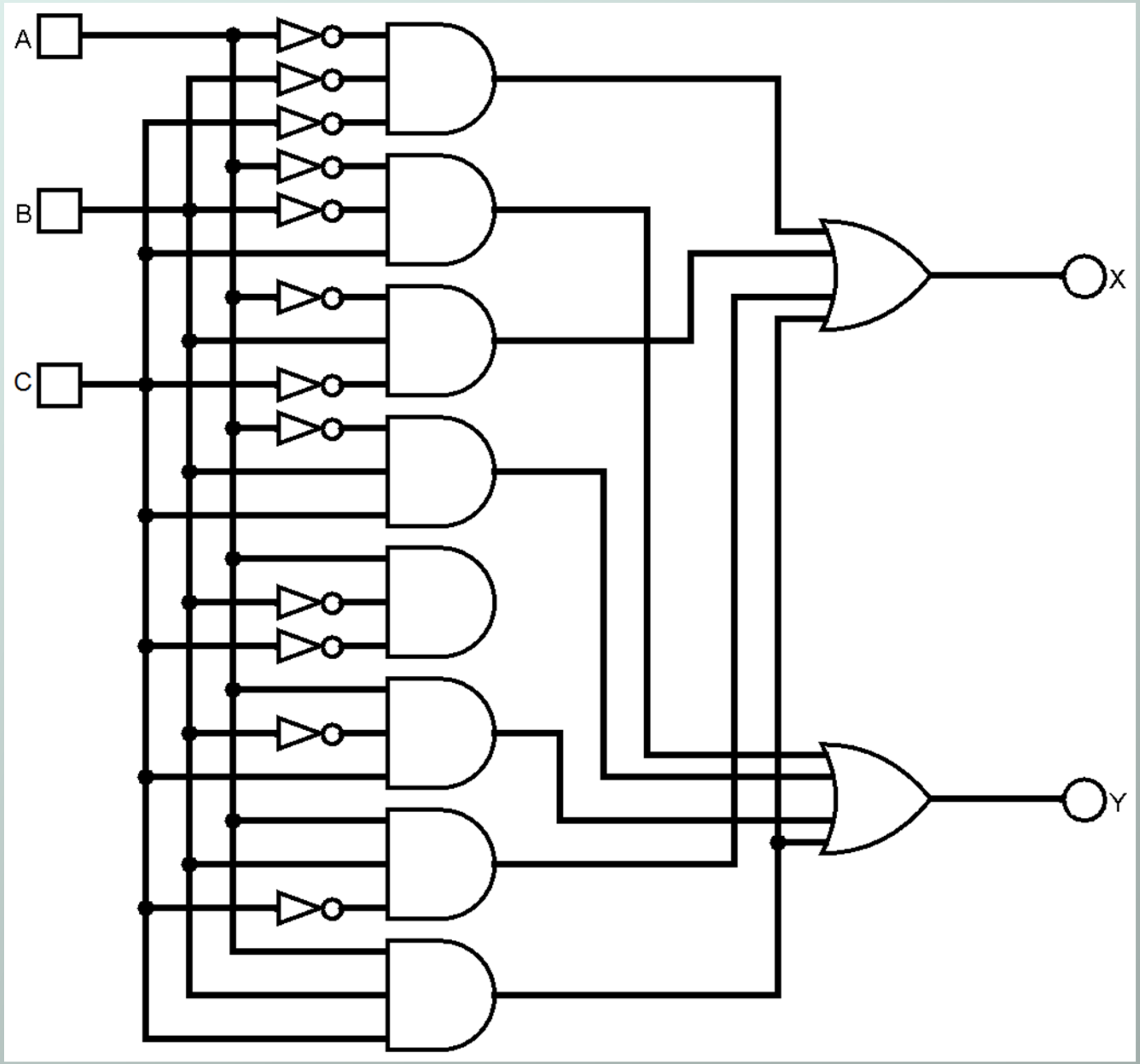
Truth Table (to circuit)

- How do we design a circuit for this?

A	B	C	X	Y
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Programmable Logic Array

- Front end is a input decode
- Back end selects outputs
- Not necessarily minimal circuit!
- Logic arrays are prebuilt



Minimization

- Using boolean algebra: combine “adjacent terms” that differ in only one variable.
- Using Karnaugh-Maps: same idea graphically.

Combinational vs. Sequential

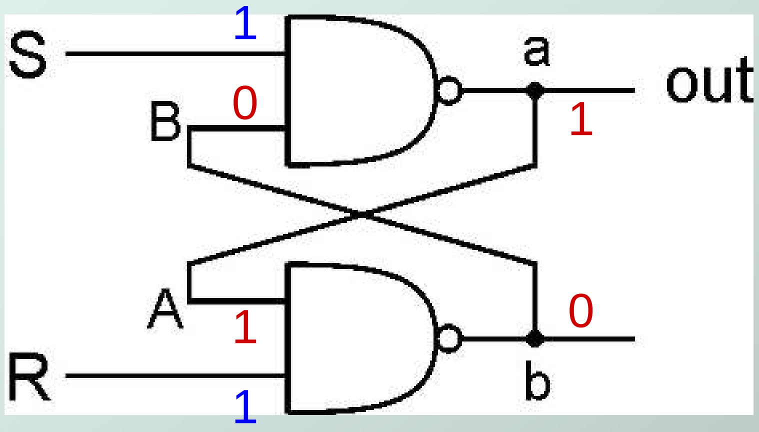
- Combinational Circuit
  - does not store information, always gives the same output for a given set of inputs
    - *example*: adder always generates sum and carry, regardless of previous inputs
- Sequential Circuit
  - stores information, output depends on stored info (state) plus input
  - so a given input might produce different outputs, depending on the stored information
  - useful for building "memory" elements and "state machines"
    - *example*: ticket counter

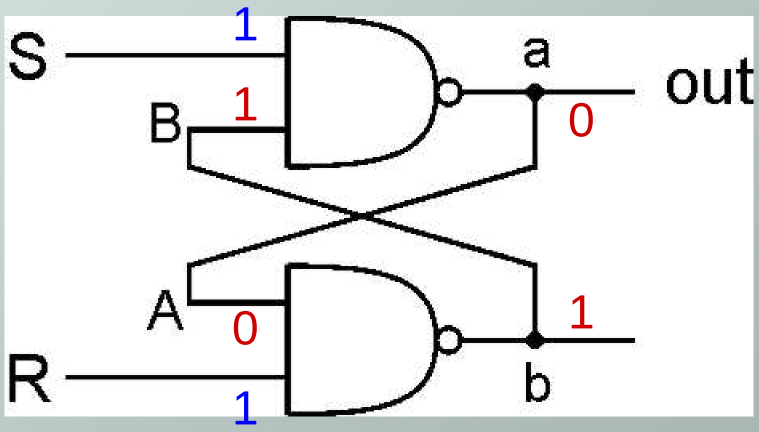
Storage elements

- 1-bit: latch, gated latch or flip-flop
- Clocked for proper timing
- Row of storage elements: register
- 2-D array: memory chip or system
- Technology:
  - Static: flip-flops using feedback (SRAMs)
  - Dynamic: charge for storage (DRAMs)

R-S Latch: Simple Storage Element

- R is used to “reset” or “clear” the element – set it to zero.
- S is used to “set” the element – set it to one.

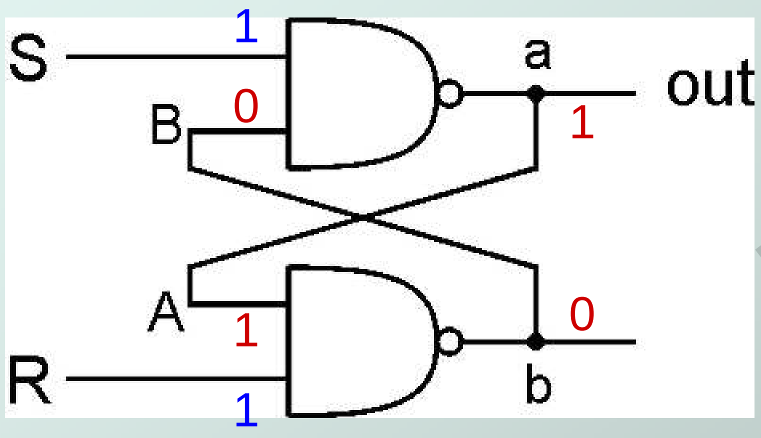




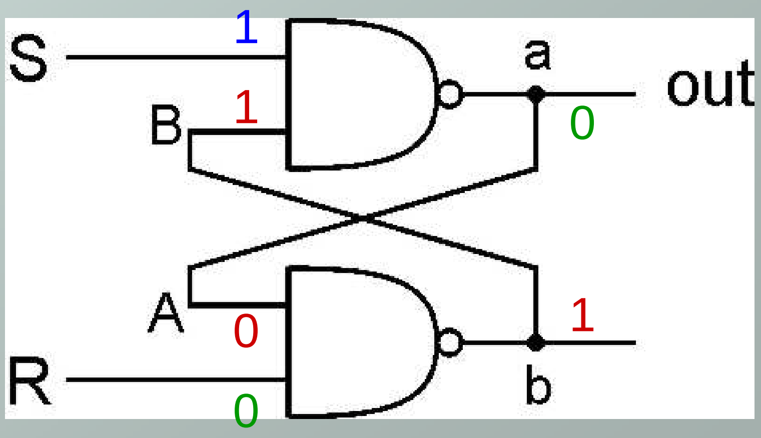
- If both R and S are one, output could be <u>either</u> zero or one.
  - “quiescent” state -- holds its previous value
  - if a is 1, b is 0, and vice versa

Clearing the R-S latch

- Suppose we start with output = 1, then change R to zero.



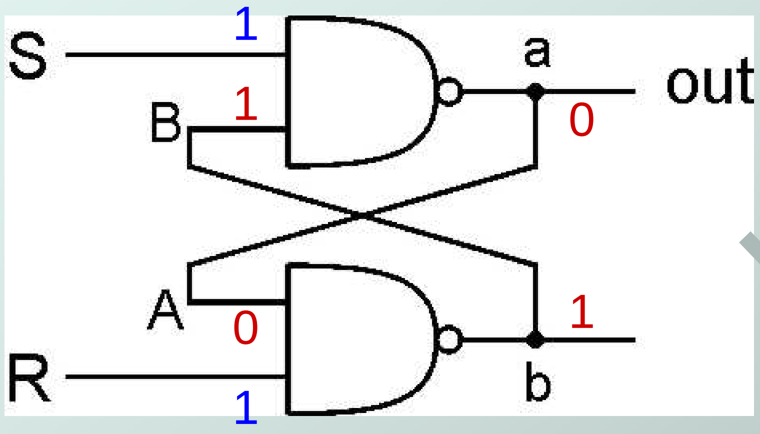
Output changes to zero.



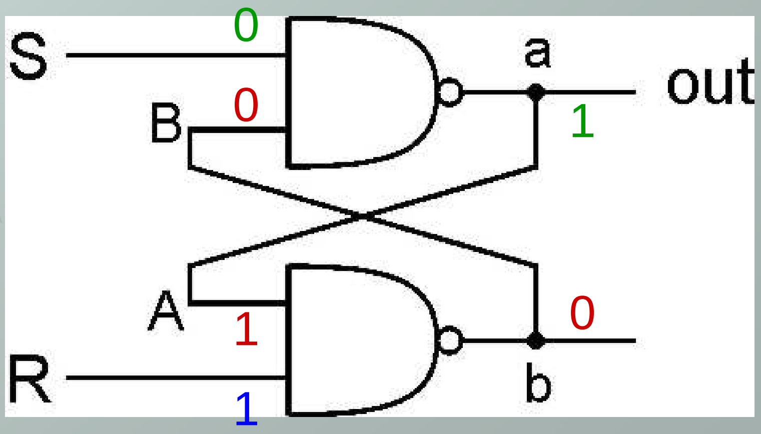
Then set R=1 to “store” value in quiescent state.

Setting the R-S Latch

- Suppose we start with output = 0, then change S to zero.



Output changes to one.



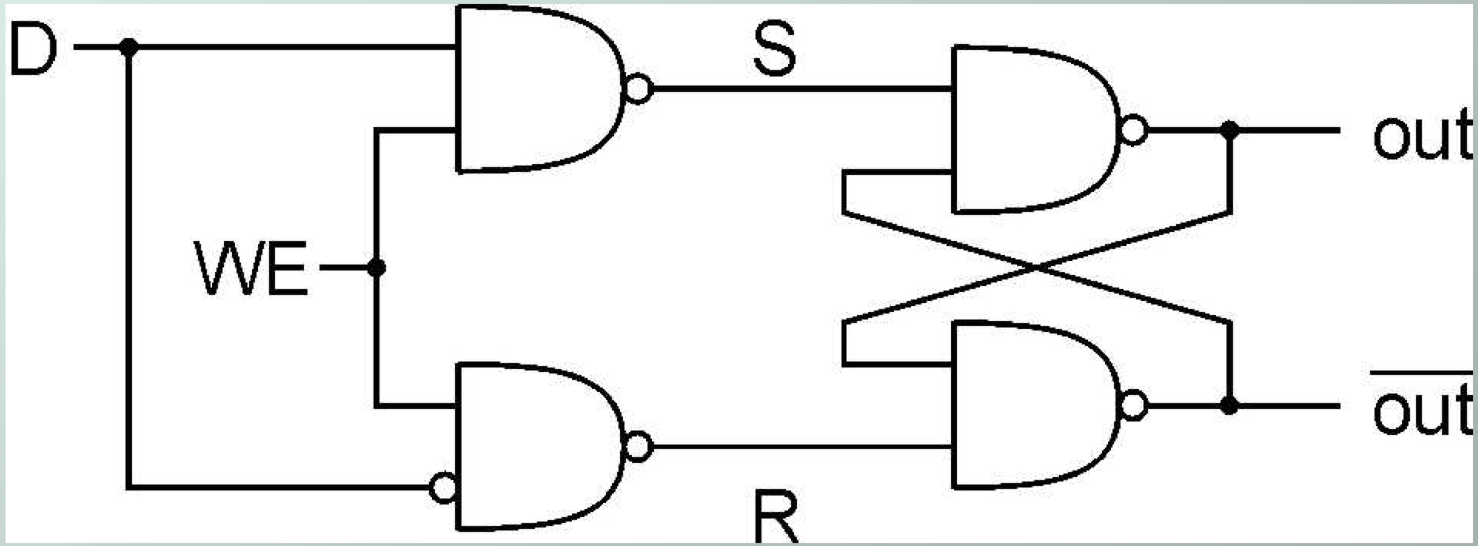
Then set S=1 to "store" value in quiescent state.

R-S Latch Summary

- **R = S = 1**
  - hold current value in latch
- **S = 0, R=1**
  - set value to 1
- **R = 0, S = 1**
  - set value to 0
- **R = S = 0**
  - both outputs equal one
  - final state determined by electrical properties of gates
  - ***Don't do it!***

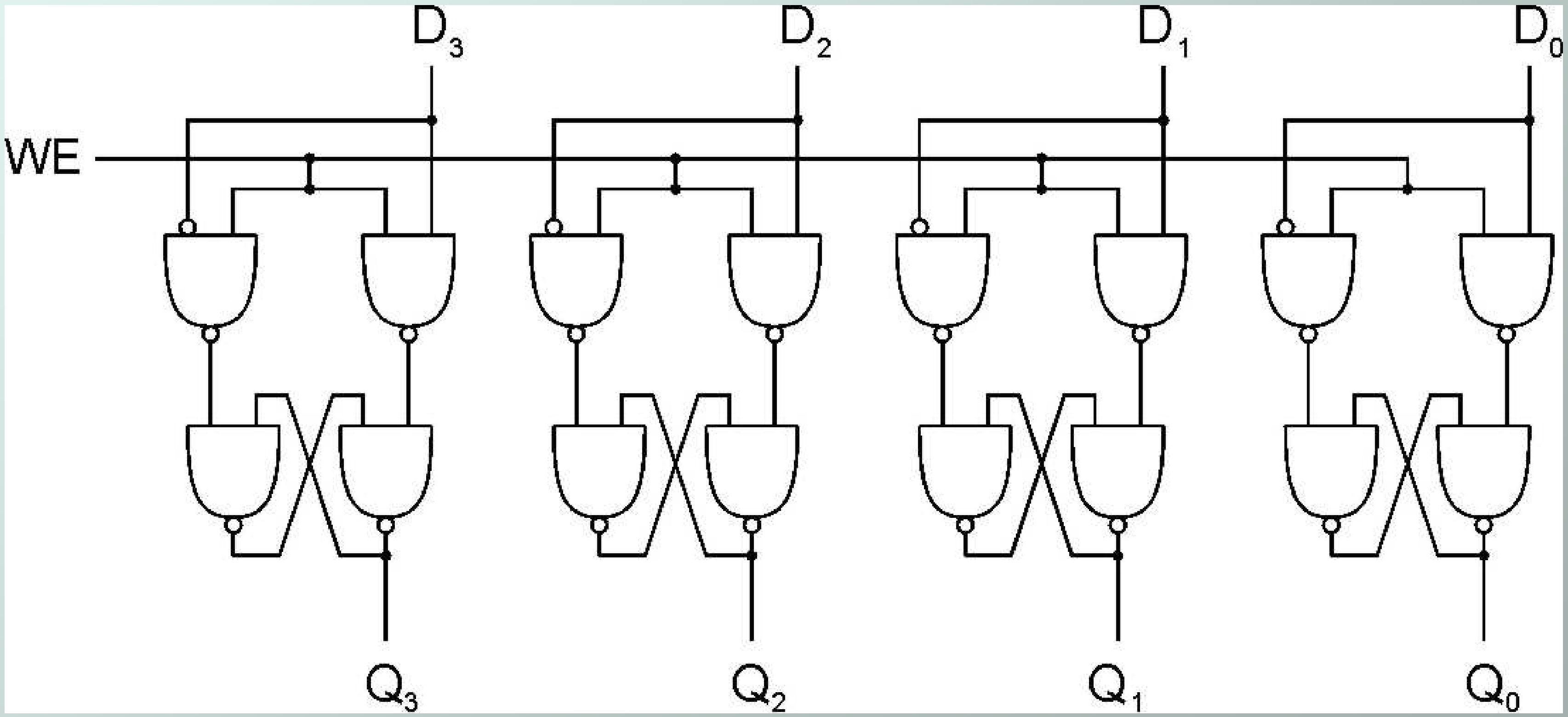
Gated D-Latch

- Two inputs: D (data) and WE (write enable)
  - when WE = 1, latch is set to value of D
    - S = NOT(D), R = D
  - when WE = 0, latch holds previous value
    - S = R = 1



Register

- A register stores a multi-bit value.
  - We use a collection of D-latches, all controlled by a common WE.



Representing Multi-bit Values

- Number bits from right (0) to left (n-1)
  - just a convention -- could be left to right, but must be *consistent*
- Use brackets to denote range:
  D[l:r] denotes bit **l** to bit **r**, from *left* to *right*

15 0

A = **0101001101010101**

A[14:9] = **101001**

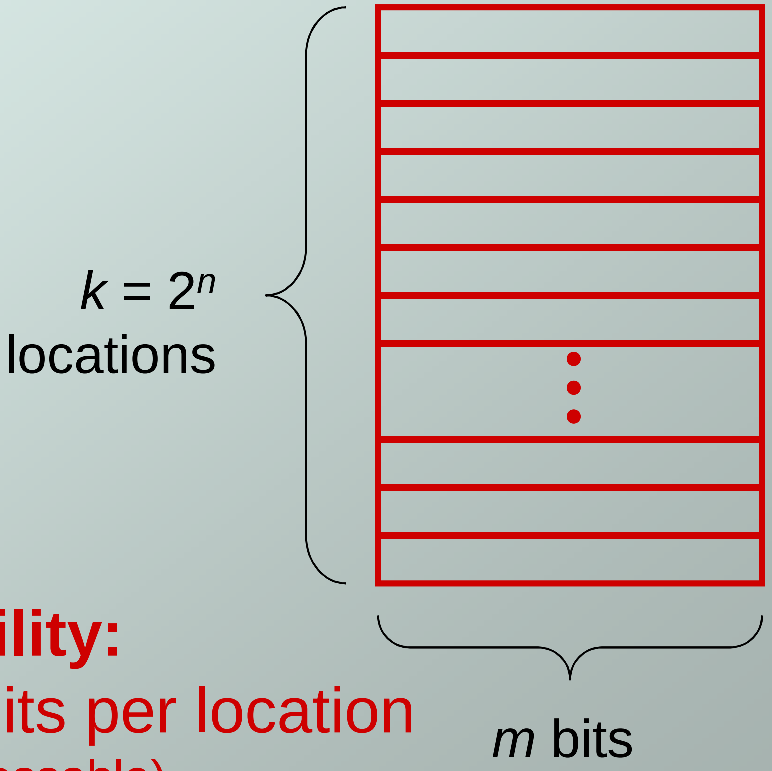
A[2:0] = **101**

- May also see A**<14:9>**,
  especially in hardware block diagrams.

Memory

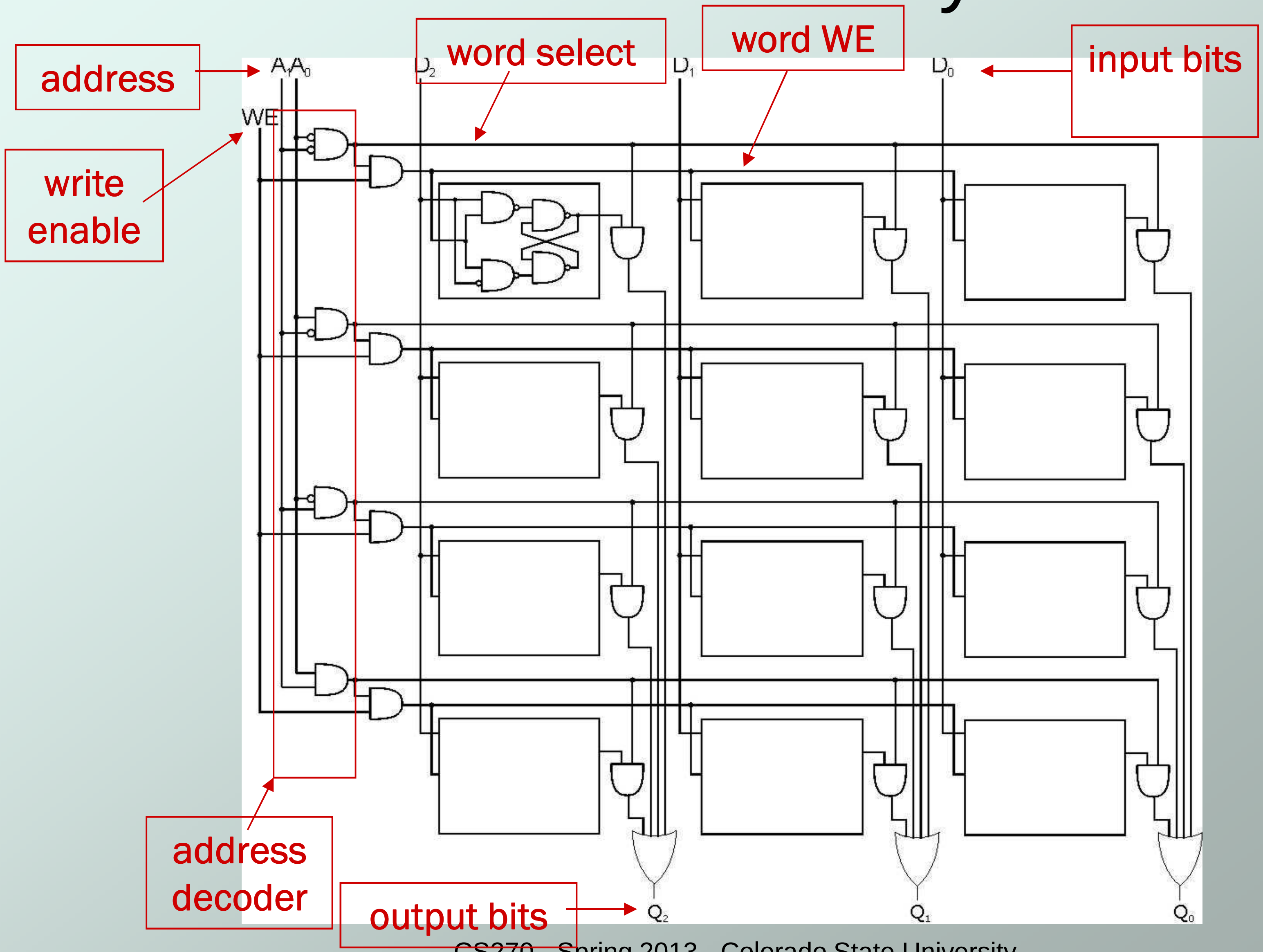
- Now that we know how to store bits,
  we can build a memory – a logical $k \times m$ array of
  stored bits.

Address Space:
number of locations
(usually a power of 2)



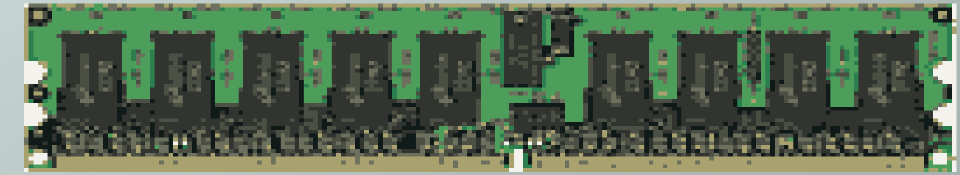
Addressability:
number of bits per location
(e.g., byte-addressable)

2^2 x 3 Memory


address
write enable
word select
word WE
input bits
address decoder
output bits
$A_1 A_0$
WE
D_2
D_1
D_0
Q_2
Q_1
Q_0

More Memory Details

- Not the way actual memory is implemented!
  - fewer transistors, denser, relies on electrical properties
- But the logical structure is very similar.
  - address decoder, word select line, word write enable
- Random Access Memory: 2 different types
  - Static RAM (SRAM)
    - fast, used for caches, maintains data when powered
  - Dynamic RAM (DRAM)
    - slower but denser, storage decays, must be refreshed
- Non-Volatile Memory: ROM, PROM, Flash



Memory Bandwidth

- Bandwidth is the rate at which memory can be read or written by the processor.
- Approximately equal to the memory bus size times the speed at which the memory is clocked.
- Examples of bandwidth (from Wikipedia):
  - Phone line, Modem, up to 5.6KB/s
  - Digital subscriber line, ADSL, up to 128KB/s
  - Wireless networking, 802.11g, up to 17.5MB/s
  - Peripheral connection, USB 2.0, 60MB/s
  - Digital video, HDMI, up to 1.275GB/s
  - Computer bus, PCI Express, up to 25.6GB/s
  - Memory chips, SDRAM, up to 52GB/s