Name _____ Date _____

CS 270 Homework 4

LC-3 Machine and ISA (due Tuesday March 6, 9:30 am in class)
No late submissions for this assignment

Homework is to be done individually.
This assignment is intended to improve your familiarity with the LC-3 instruction set architecture, and for you to understand how each of the instructions in the machine is implemented in a cycle-by-cycle manner. We will make use of the LC-3Viz tool, but be aware that it may have a few bugs an inaccuracies. You will also develop familiarity with the register transfer notation.

Recap

The *Register Transfer Notation*, also called a description at the *Register Transfer Level* (RTL) is a precise description of the behavior of large, complicated digital designs, often called *data paths* with a notation that is slightly "higher-level" than a circuit level. It is typically used to describe designs *cycle by cycle* (also called a *cycle accurate* description).

A data-path consists of storage elements (registers and memories) connected by combinational logic (muxes, operators, wires and possibly, busses). At each clock cycle, a number of register-to-register *tansfers* can take place. The designer's job is as follows:

- First specify clearly which transfers should take place in what order (i.e., at each clock cycle), and under what conditions. The current version of LC3Viz is nothing but a flash animation of this.
- Next, specify which control signals should be active (i.e., "high," "on" or 1) for these transfers to actually happen.
- Design an FSM that issues these control signals at the right time and under the right conditions.

In this assignment, we will take a close look at the first two steps. You will first fill out a table giving a cycle by cycle description of the transfers that must happen in the LC-3 in order for it to achieve the desired behavior. Next, you will identify the signals that must be active in order for these desired transfers to take place.

Cycle	Transfers	Control Signals
1	MAR ← PC	GatePC, LD.MAR
2	MDR ← Mem[MAR]; PC ← PC+1	Mem.EN, LD.MDR, PCMUX.Sel = 10, LD.PC
3	IR ← MDR	Gate.MDR, LD.IR

Table 1: RTL Description of the Instruction Fetch Phase and the control signals in each clock cycle that accomplish the desired transfers.

Illustration We will describe the two steps for the three cycles of the execution of every LC-3 instruction, namely the *instruction fetch* phase. In Table 1, the middle section describes the transfers desired, and the right section specifies the control signals to accomplish the transfer. The left arrow is to be read like an "assignment" or a transfer, and we use right brackets to denote memory references, e.g., **`Mem[0x3000]`** denotes the content of memory at adress **`0x3000`**, and **`Mem[PC]`** denotes the contents of memory at a location whose address is in the PC.

Your job is to fill out similar tables for all the remaining cycles of all the instructions, using LC3Viz as a study guide.

Cycle	Transfers	Control Signals
4		

Table 2: Cycle 4 of Register ADD

Cycle	Transfers	Control Signals
4		

Table 3: Cycle 4 of Immediate ADD

Cycle	Transfers	Control Signals
4		

Table 4: Cycle 4 of Register AND

Cycle	Transfers	Control Signals
4		

Table 5: Cycle 4 of Immediate ADD

Cycle	Transfers	Control Signals
4		

Table 6: Cycle 4 of NOT

Cycle	Transfers	Control Signals
4		

Table 7: Cycle 4 of BR

Cycle	Transfers	Control Signals
4		

Table 8: Cycle 4 of JMP

Cycle	Transfers	Control Signals
4		

Table 9: Cycle 4 of LEA

Cycle	Transfers	Control Signals
4		
5		
6		

Table 10: Cycles 4–6 of LD

Cycle	Transfers	Control Signals
4		
5		
6		

Table 11: Cycle 4–6 of LDR

Cycle	Transfers	Control Signals
4		
5		
6		
7		
8		

Table 12: Cycle 4–8 of LDI

Cycle	Transfers	Control Signals
4		
5		
6		

Table 13: Cycles 4–6 of ST

Cycle	Transfers	Control Signals
4		
5		
6		

Table 14: Cycle 4–6 of STR

Cycle	Transfers	Control Signals
4		
5		
6		
7		
8		

Table 15: Cycle 4–8 of STI