Name: _____ **Date:** _____

CS270 Homework Assignment 2 (HW2)

Due Thursday, Feb 9 (start of class)
Homework and programming assignments are to be done individually.

Goals

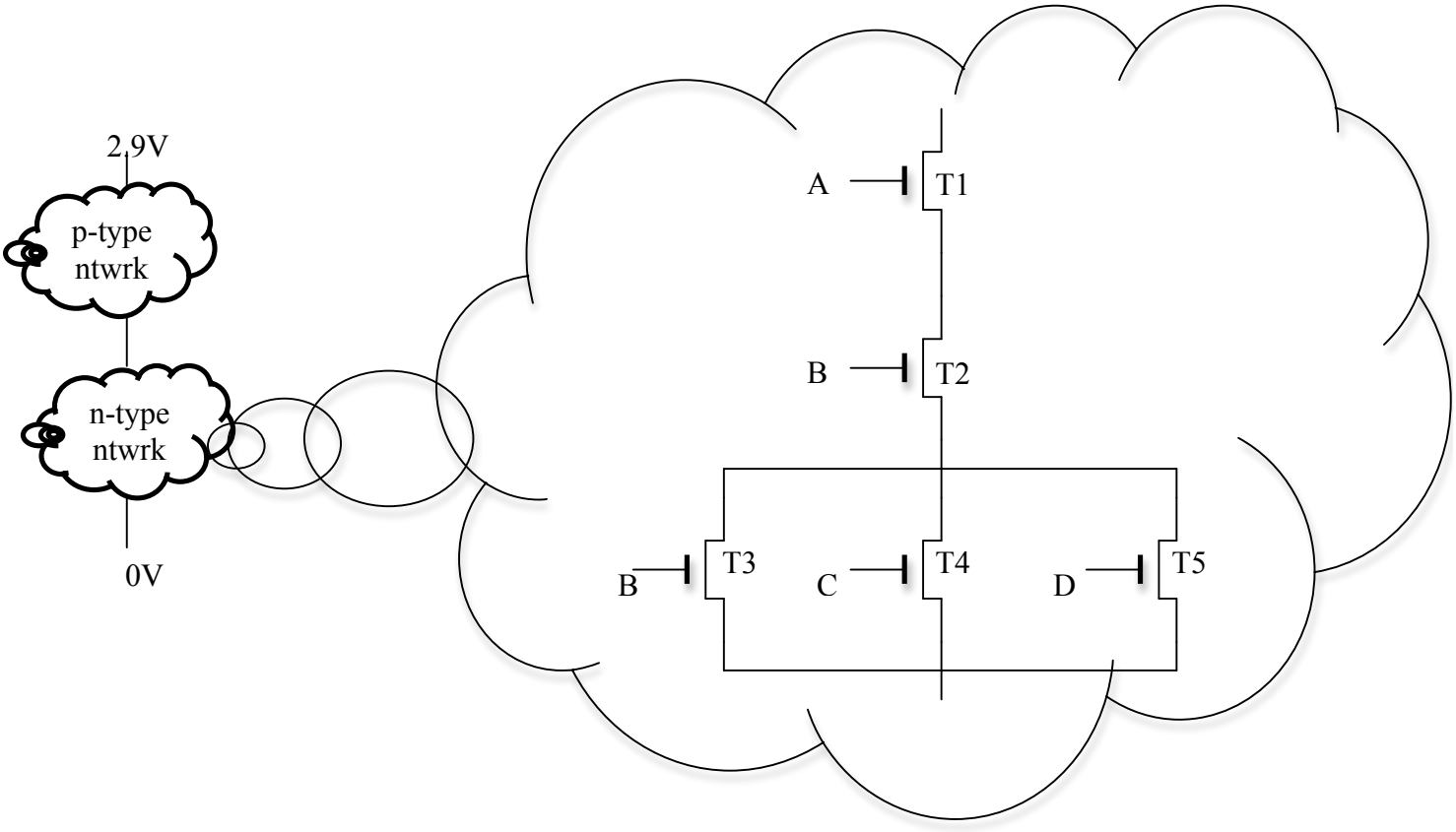
To understand transistor basics, logic gates (NOT, NAND, NOR), DeMorgan's Law, decoders, multiplexers, and combinational logic. This assignment requires the use of a logic simulator called Logisim, which will be explained in class and practiced in the recitation. The Logisim web page, tutorial, and software is linked to the class web page. To run the Logisim software, change to directory containing the .jar file and type the following: **$ java -jar logisim-2.1.0.jar**

The Assignment

Question 1 (10 points): A transistor is a device where the voltage on the gate controls a "switch" between the drain and source. Fill in the table below that specifies the transistor state based on the type of the transistor (n-type or p-type) and the voltage at the gate with the words 'open' or 'closed'

Input	*n-type*	*p-type*
0		
1		

Question 2 (40 points): The following question concerns series-parallel circuits described in the lecture on Feb 12. The material is not covered in the book, so please study the class notes and/or come to office hours. Consider the n-type network in the circuit below.



Fill up the truth table below [15 pts] under the following assumptions:

1. Whenever there is a path from the output to ground, the output is 0
2. For all other combinations, assume that somehow, the output will "automagically" become 1.

A	*B*	*C*	*D*	*T1*	*T2*	*T3*	*T4*	*T5*	*Out*
0	*0*	*0*	*0*	**open**					
0	*0*	*0*	*1*	**open**					
0	*0*	*1*	*0*						
0	*0*	*1*	*1*						
0	*1*	*0*	*0*						
0	*1*	*0*	*1*		**closed**	**closed**			
0	*1*	*1*	*0*						
0	*1*	*1*	*1*						
1	*0*	*0*	*0*						
1	*0*	*0*	*1*						
1	*0*	*1*	*0*						
1	*0*	*1*	*1*						
1	*1*	*0*	*0*						
1	*1*	*0*	*1*						
1	*1*	*1*	*0*						
1	*1*	*1*	*1*						

Now draw the p-type complementary circuit will connect the output to Vdd (2.9V) [15 pts].

Does your complete circuit provide a simultaneous path from 2.9V to ground for any input combination? If so, which one(s)? [4 pts]

Is there some input combination for which the output is "floating" (i.e., connected to neither of 2.9V or ground)? [4 pts]

Based in this, is this a well-designed circuit? ? [2 pt]

Question 3 (10 points):

Wikipedia describes De Morgan's laws (http://en.wikipedia.org/wiki/De_Morgan%27s_laws):
In formal logic, De Morgan's laws are rules relating the logical operators "and" and "or" in terms of each other via negation, namely:

NOT (P OR Q) = (NOT P) AND (NOT Q)
NOT (P AND Q) = (NOT P) OR (NOT Q)

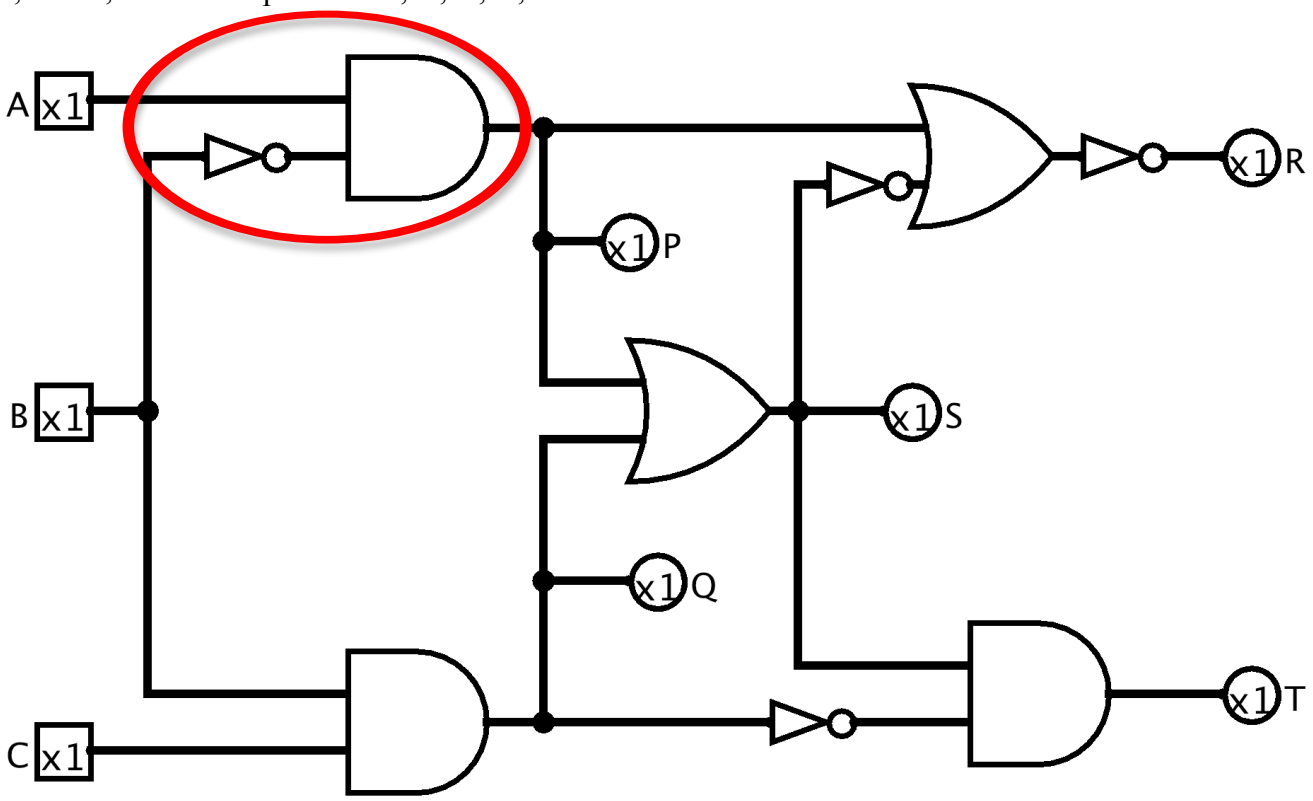
Fill in the truth table below that summarizes the first law shown above.

P	*Q*	*P* OR *Q*	*NOT(P* OR *Q)*	*NOT P*	*NOT Q*	*(NOT P)* AND *(NOT Q)*
0	*0*				**1**	
0	*1*	**1**				
1	*0*			**0**		
1	*1*					**0**

Question 4 (15 points): Design a 4-input, 1-output multiplexer using Logisim, and turn in a schematic and fill in the truth table. How many control lines are required?

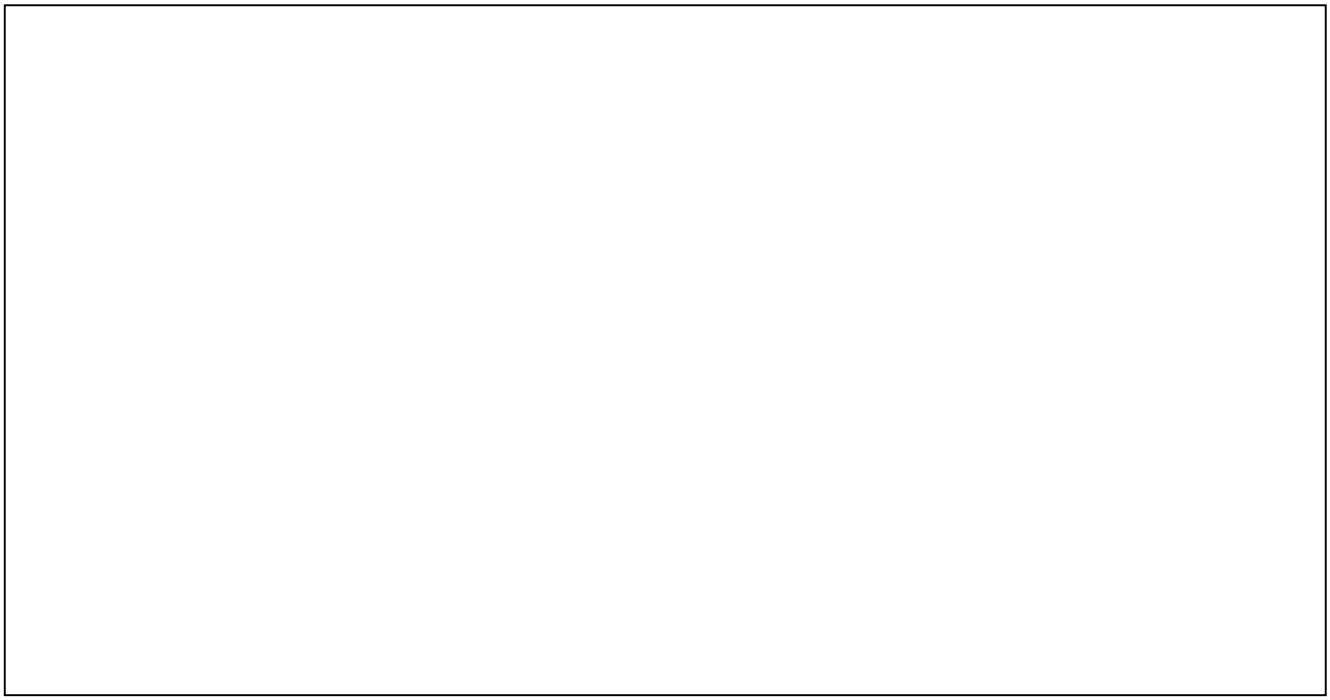
InputA	*InputB*	*InputC*	*InputD*	*Select1*	*Select0*	*Output*
0	***x***	***x***	***x***	**0**	**0**	**0**
1	***x***	***x***	***x***	**0**	**0**	
x	***0***	***x***	***x***	**0**	**1**	
x	***1***	***x***	***x***	**0**	**1**	
x	***x***	**0**	***x***	**1**	**0**	
x	***x***	**1**	***x***	**1**	**0**	
x	***x***	***x***	**0**	**1**	**1**	
x	***x***	***x***	**1**	**1**	**1**	

Question 5 (25 points): Fill in the truth table for the following combinational circuit. The inputs are A, B, and C, and the outputs are M, N, O, X, and Y.



A	*B*	*C*	*P*	*Q*	*R*	*S*	*T*
0	*0*	*0*					
0	*0*	*1*		**0**			
0	*1*	*0*	**0**				**0**
0	*1*	*1*					
1	*0*	*0*			**0**		
1	*0*	*1*					
1	*1*	*0*					
1	*1*	*1*				**1**	

Now apply De-Morgan's laws to change the part of the circuit that is in the red oval, design the modified circuit in Logisim and turn in the schematic, and its new truth table.



Submission Instructions

All homework assignments must be handed in at the beginning of class on the due date. Logisim can save circuits as .gif pictures, please submit a picture for each circuit. After printing your circuits, you can cut and paste to this document, or attach to the back with a label showing the question number.

Late Policy

Late assignments will be accepted up to 48 hours past the due date and time. There will be a penalty of 10% for each delay by 24 hours. Assignments will not be accepted past the 48 hour delay. Late submissions should be made via RamCT, or by delivering the paper copy to the CS front desk where they will timestamp the submission.