1) What is the range of values for the PC offset for the following instructions: JMP, LEA, STI?

2) What information is stored in the Processor Status Register? what bit locations hold this information?

3) What does the JMP R2 instruction do? How is this different from the RET instruction?

4) What is PC offset for the following BR instruction? Now show the 16 bits that make up the BR instruction.

```
        BRz data1
        ADD R2, R2, #5
        JSRR R4
data1   .FILL 0x1234
```

5) Given the following information what will be the value in the PC after the following instruction TRAP x23, What is the first instruction executed by the TRAP routine?

location	data
x0020	x0420
x0021	x0251
x0022	x046C
x0023	x0326
x0024	x0324

location	data
x0230	x2A43
x0231	x32AC
x0232	x5E1F
x0233	x8FB2
x0234	xE8A1

location	data
x0323	xFADC
x0324	x32AC
x0325	xAE1F
x0326	x330F
x0327	x98A1

6) What change signifies that the keyboard is in interrupt vs polling mode?

7) What is the difference between the frame pointer and the stack pointer?

8) List the 10 parts on the stack protocol in order. What parts have to be done by the caller or callee, and what parts were a choice made by the protocol designer?

9) What do the following instructions have in common? LDI, LDR, STI, STR, JSRR, JMP, RET

10) What instructions make up a PUSH? What instructions make up a POP?

11) If the LC3 had 32 registers how would the ADD instruction be affected?

12) How many times does the LDR instruction access memory? What about STI? What about TRAP?

13) What is the purpose of bit 15 int the KBSR? Bit 14?

14) Besides an interrupt signal what else does the interrupting device need to send the LC3 processor for an interrupt to be handled?