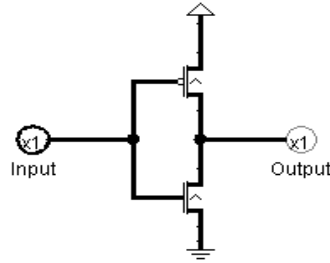


Fill in the truth tables and draw the following gates, a NOT gate is shown for reference:

A	O
1	0
0	1



**2 input NOR**

A	B	O
0	0	1
0	1	0
1	0	0
1	1	0

**3 input NAND**

A	B	C	O
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

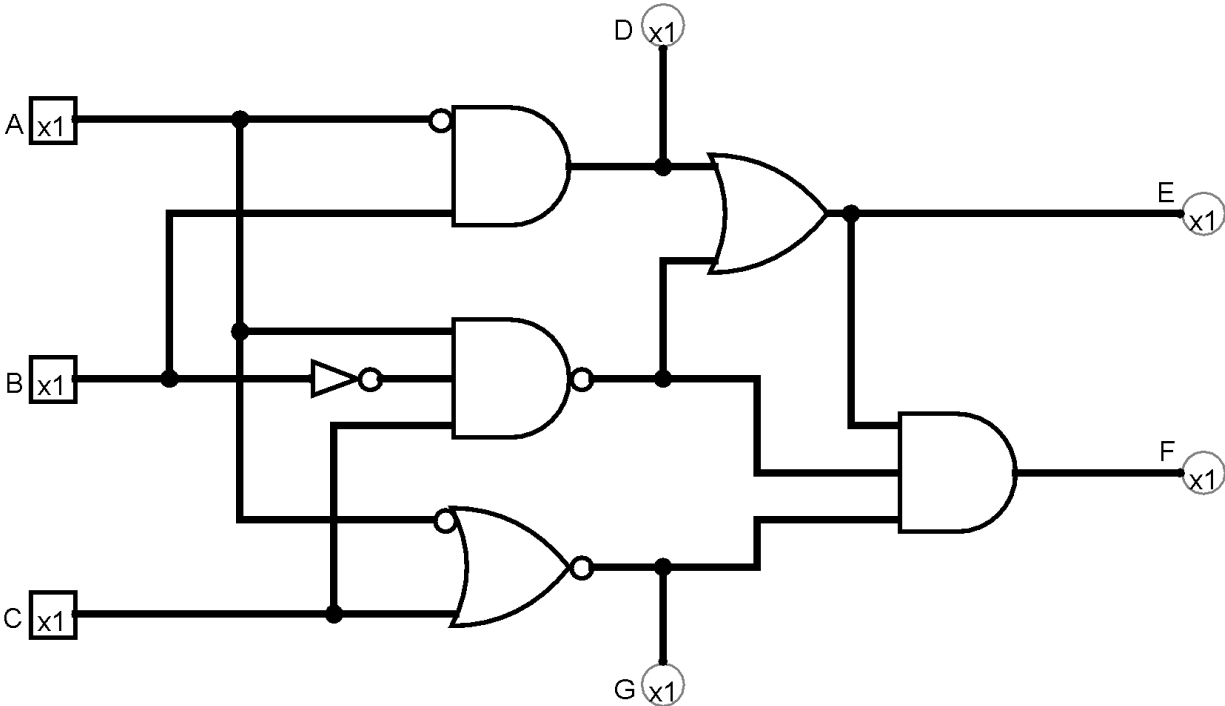
**3 input OR**

A	B	C	O
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

**2 input AND**

A	B	O
0	0	0
0	1	0
1	0	0
1	1	1

Complete the partial truth table for the following circuit:



Truth Table						
A	B	C	D	E	F	G
1	1	1	0	1	0	0
0	1	0	1	1	0	0
1	0	0	0	1	1	1