

1) Define the following terms [For definitions see slides / Chapter 5 pdf / Wikipedia / Google](#)

Cache:

Direct Mapped:

Tag:

Associativity:

Write back cache:

Write through cache:

Allocate on miss:

Compulsory miss:

Capacity miss:

Conflict miss:

Valid bit:

Dirty bit:

2) Given a 32 KB (2^{15} bytes exactly) direct-mapped cache with a 64 byte block size, byte addressing, and 32 bit addresses, answer the following questions.

a) Number of offset bits?

64 addresses per block so 6 bits used for offset

b) Number of index bits?

2^{15} Bytes / 64 Bytes per line = 512 lines, so 9 bits to index all lines

c) Number of tag bits?

32 bit addresses - 6 bit offset - 9 bits of index = 17 bits for tag

d) What index will the following address be mapped to 0xFA86A3D7 ?

Convert to binary: 0b11111010100001101010001111010111 then select index bits (6 – 14)
so index is 0b010001111 or 143

e) What tag will be associated with the above address?

tag is the most significant 17 bits so 11111010100001101

f) What extra bit of information will be needed if the cache is a write back cache?

Dirty bit

g) How many index bits will be needed if the cache is changed to a 2 way associative cache?

2 way associative means number of indexes is cut in half so 256 locations or 8 index bits

h) How many index bits will be needed if the cache is changed to a fully associative cache?

Fully associative means no index is required so 0 bits

i) How many tag comparators will be needed if the cache is changed to an 8 way associative cache?

8 way associative means data from a specific memory location could be in one of 8 locations
so 8 comparators will be needed.