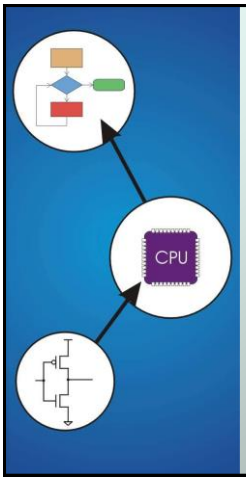
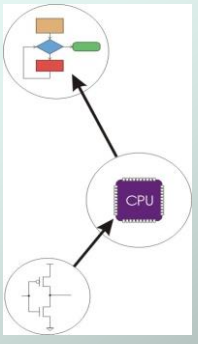


Chapter 3
Digital Logic Structures

Original slides from Gregory Byrd, North Carolina State University

Modified slides by Chris Wilcox, Colorado State University

Computing Layers



Problems

Algorithms

Language

Instruction Set Architecture

Microarchitecture

Circuits

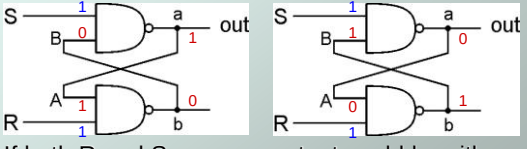
Devices

Combinational vs. Sequential

- **Combinational Circuit**
  - does not store information, always gives the same output for a given set of inputs
    - *example*: adder always generates sum and carry, regardless of previous inputs
- **Sequential Circuit**
  - stores information, output depends on stored info (state) plus input
  - so a given input might produce different outputs, depending on the stored information
  - useful for building "memory" elements and "state machines"
    - *example*: ticket counter

R-S Latch: Simple Storage Element

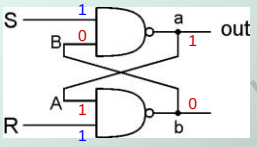
- R is used to "reset" or "clear" the element – set it to zero.
- S is used to "set" the element – set it to one.



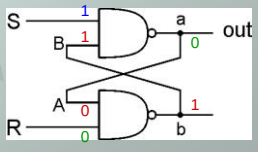
- If both R and S are one, output could be either zero or one.
  - "quiescent" state -- holds its previous value
  - if a is 1, b is 0, and vice versa

Clearing the R-S latch

- Suppose we start with output = 1, then change R to zero.



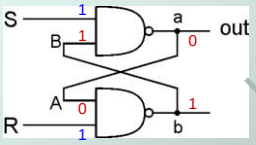
Output changes to zero.



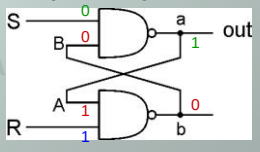
Then set R=1 to "store" value in quiescent state.

Setting the R-S Latch

- Suppose we start with output = 0, then change S to zero.



Output changes to one.



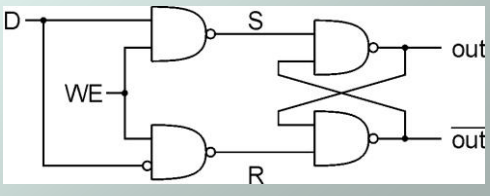
Then set S=1 to "store" value in quiescent state.

R-S Latch Summary

- **R = S = 1**
  - hold current value in latch
- **S = 0, R=1**
  - set value to 1
- **R = 0, S = 1**
  - set value to 0
- **R = S = 0**
  - both outputs equal one
  - final state determined by electrical properties of gates if you transition to R = S = 1.
  - ***Don't do it!***

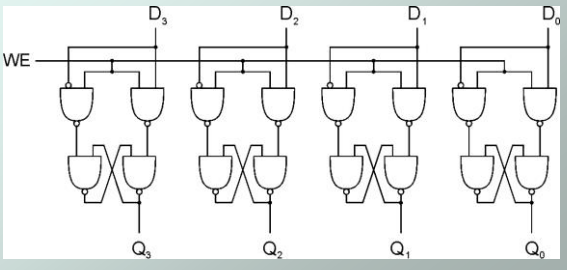
Gated D-Latch

- Two inputs: D (data) and WE (write enable)
  - when **WE = 1**, latch is set to **value of D**
    - S = NOT(D), R = D
  - when **WE = 0**, latch holds **previous value**
    - S = R = 1



Register

- A register stores a multi-bit value.
  - We use a collection of D-latches, all controlled by a common WE.

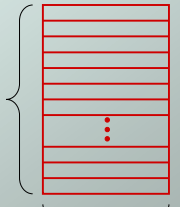


Memory

- Now that we know how to store bits, we can build a memory – a logical $k \times m$ array of stored bits.

Address Space:
number of locations
(usually a power of 2)

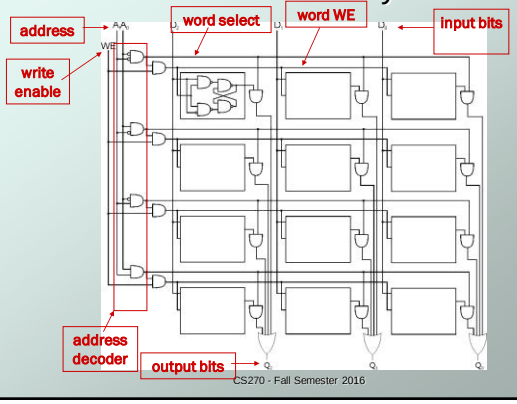
$k = 2^n$ locations



Addressability:
number of bits per location
(e.g., byte-addressable)

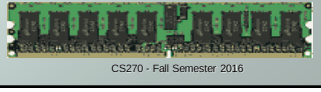
m bits

2^2 x 3 Memory



More Memory Details

- Not the way actual memory is implemented!
  - fewer transistors, denser, relies on electrical properties
- But the logical structure is very similar.
  - address decoder, word select line, word write enable
- Random Access Memory: 2 different types
  - **Static RAM** (SRAM)
    - fast, used for caches, maintains data when powered
  - **Dynamic RAM** (DRAM)
    - slower but denser, storage decays, must be refreshed
- Non-Volatile Memory: **ROM, PROM, Flash**



Memory Bandwidth

- Bandwidth is the rate at which memory can be read or written by the processor.
- Approximately equal to the memory bus size times the speed at which the memory is clocked.
- Examples of bandwidth (from Wikipedia):
  - Phone line, Modem, up to 5.6KB/s
  - Digital subscriber line, ADSL, up to 128KB/s
  - Wireless networking, 802.11g, up to 17.5MB/s
  - Peripheral connection, USB 2.0, 60MB/s
  - Digital video, HDMI, up to 1.275GB/s
  - Computer bus, PCI Express, up to 25.6GB/s
  - Memory chips, SDRAM, up to 52GB/s