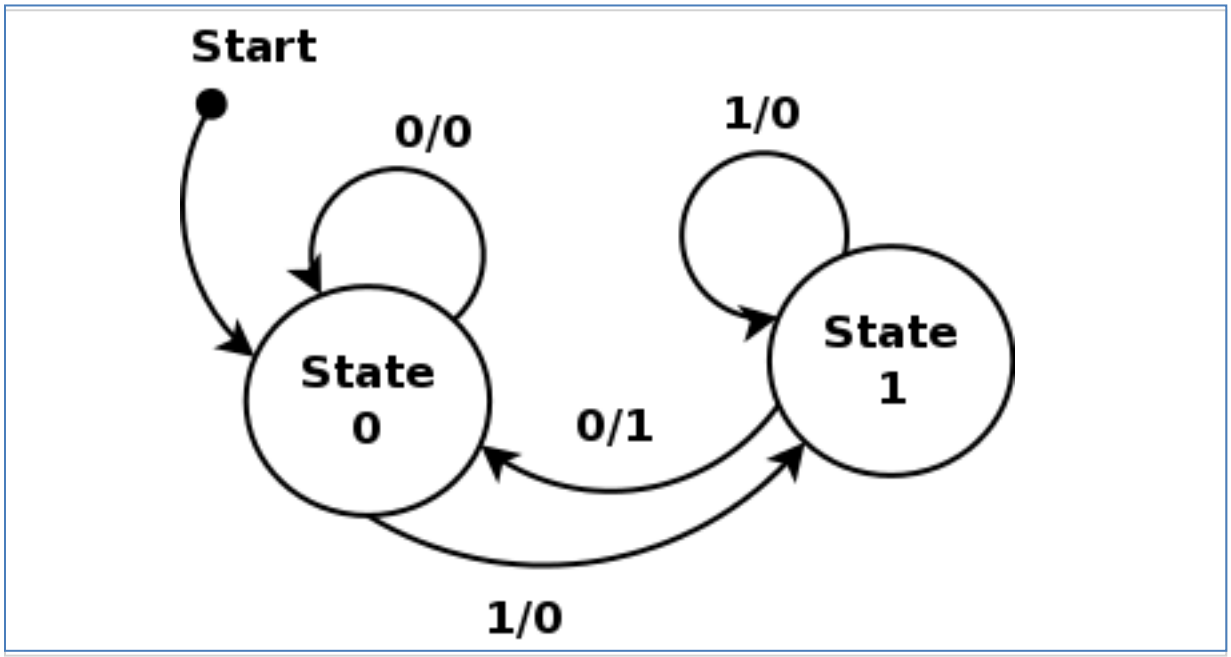
CS270 Recitation 12
"Help Session for State Machine"

Goals: Design a Logisim circuit that implements the simple state machine shown below:



Here are a few clarifications that may help you, and questions you should be able to answer:

- What is the sequence of bits that is detected by this state machine?
- The state should be stored in D-latches. How many do you need (minimum number)?
- The truth table is combinational logic similar to what you have already done.
- You must use a D-latch the output, since it's on a transition.
- For this recitation, optimization is allowed and encouraged. The fewer gates the better!

Input	*Current State*	*Output*	*Next State*
0	*0*		
0	*1*		
1	*0*		
1	*1*		