

The diagram on the left shows three circles. The bottom circle contains a logic gate symbol. An arrow points from it to the middle circle, which contains a purple square labeled 'CPU'. Another arrow points from the middle circle to the top circle, which contains a more complex logic diagram with various colored blocks and lines.

Chapter 3 Digital Logic Structures

Original slides from Gregory Byrd, North Carolina State University
Modified by Chris Wilcox, Sanjay Rajopadhye Colorado State University

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Computing Layers

The diagram on the left is identical to the one in the first slide, showing the progression from logic gates to a CPU to a higher-level logic structure.

- Problems
-
- Algorithms
-
- Language
-
- Instruction Set Architecture
-
- Microarchitecture
-
- Circuits
-
- Devices ←

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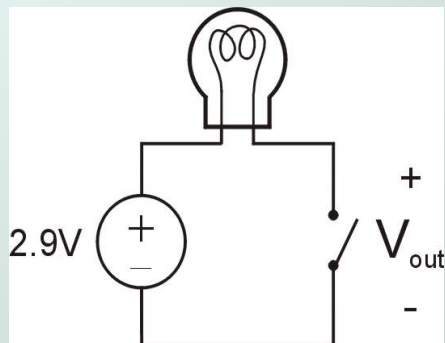
Transistor: Building Block of Computers

- Microprocessors contain billions of transistors
 - Intel Pentium 4 (2000): 48 million
 - IBM PowerPC 750FX (2002): 38 million
 - IBM/Apple PowerPC G5 (2003): 58 million

Logically, each transistor acts as a switch

- Combined to implement logic functions (gates)
 - AND, OR, NOT
- Combined to build higher-level structures
 - Adder, multiplexer, decoder, register, memory, ...
- Combined to build processor
 - LC-3

Simple Switch Circuit



- Switch **open**:
 - Open circuit, no current
 - Light is **off**
 - V_{out} is **+2.9V**
- Switch **closed**:
 - Short circuit across switch, current flows
 - Light is **on**
 - V_{out} is **0V**

Switch-based circuits can easily represent two values:
on/off, open/closed, voltage/no voltage.

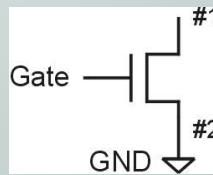
n-type Transistor

● A transistor is an **electrically** controlled switch

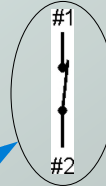
● n-type

- when Gate has **positive** voltage, short circuit between #1 and #2 (switch **closed**)
- when Gate has **zero** voltage, open circuit between #1 and #2 (switch **open**)

Terminal #2 is connected to GND (0V).



Gate = 1



Gate = 0

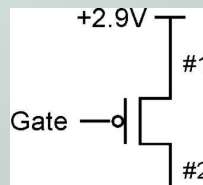


p-type Transistor

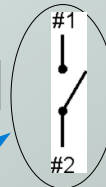
● p-type is *complementary* to n-type

- when Gate has **positive** voltage, open circuit between #1 and #2 (switch **open**)
- when Gate has **zero** voltage, short circuit between #1 and #2 (switch **closed**)

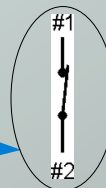
Terminal #1 is connected to +2.9V.



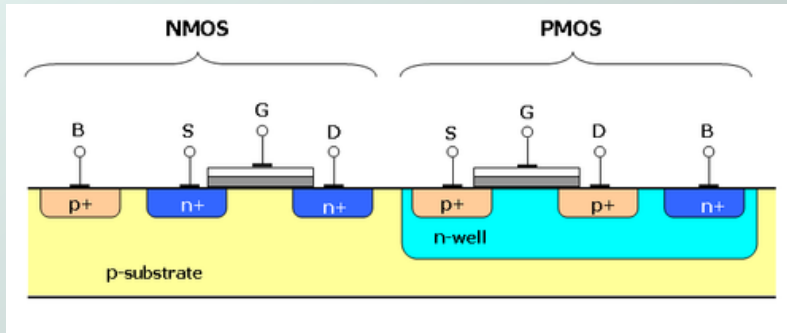
Gate = 1



Gate = 0



Physical Transistor



<http://en.wikipedia.org/wiki/CMOS>

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Logic Gates

- ◆ Use switch behavior of MOS transistors to implement logical functions: AND, OR, NOT.
- ◆ Digital symbols:
 - recall that we assign a range of analog voltages to each digital (logic) symbol



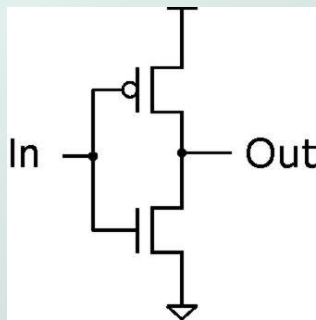
- assignment of voltage ranges depends on electrical properties of transistors being used
 - ◆ typical values for "1": +5V, +3.3V, +2.9V
 - ◆ from now on we'll use +2.9V

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CMOS Circuit

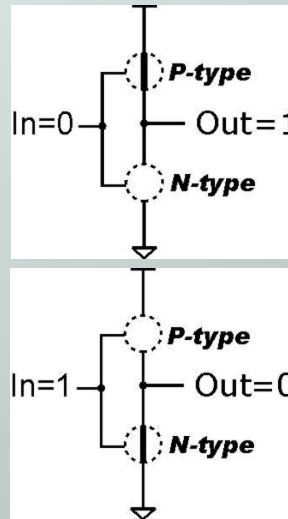
- ◆ **Complementary** MOS
- ◆ Uses both **n-type** and **p-type** MOS transistors
 - p-type
 - ◆ Attached to + voltage
 - ◆ Pulls output voltage UP when input is zero
 - n-type
 - ◆ Attached to GND
 - ◆ Pulls output voltage DOWN when input is one
- ◆ **For all inputs, make sure that output is either connected to GND or to +, but not both!**

Inverter (NOT Gate)

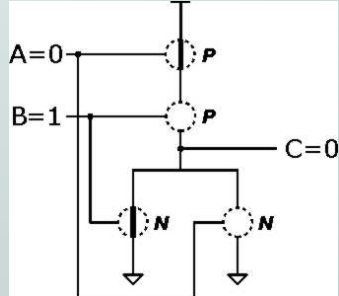
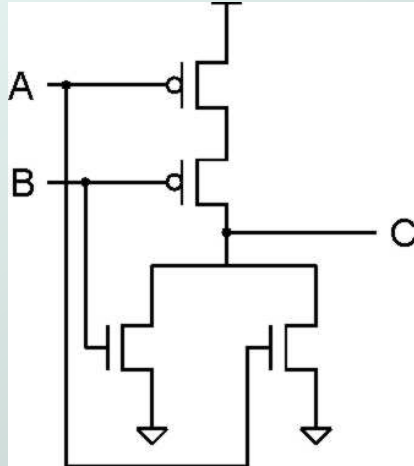


In	Out	In	Out
0 V	2.9 V	0	1
2.9 V	0 V	1	0

Truth table



NOR Gate

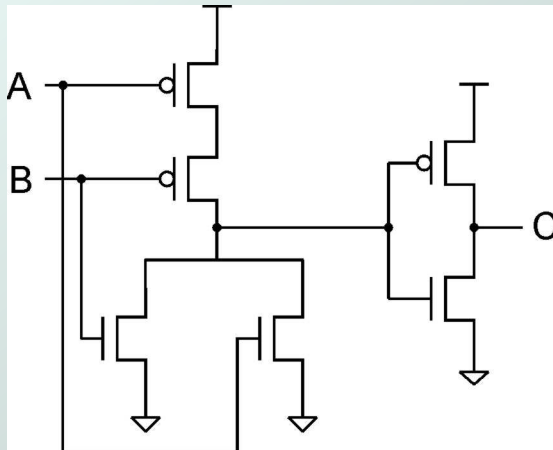


A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Truth table

Note: Serial structure on top, parallel on bottom.

OR Gate

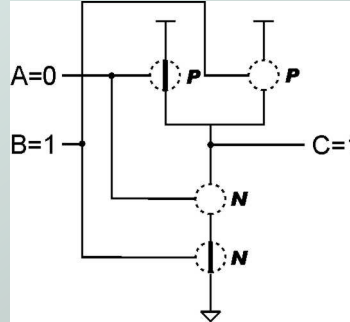
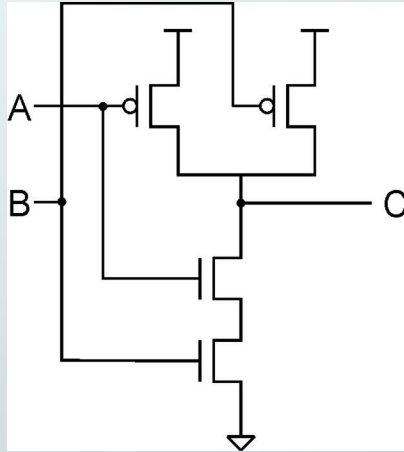


A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Truth table

Add inverter to NOR.

NAND Gate (AND-NOT)

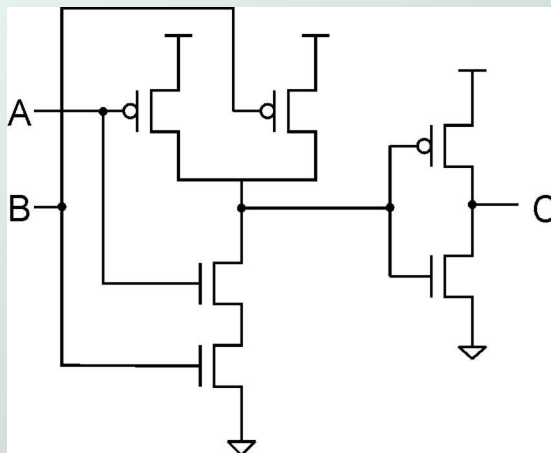


Truth table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Note: Parallel structure on top, serial on bottom.

AND Gate



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

Add inverter to NAND.

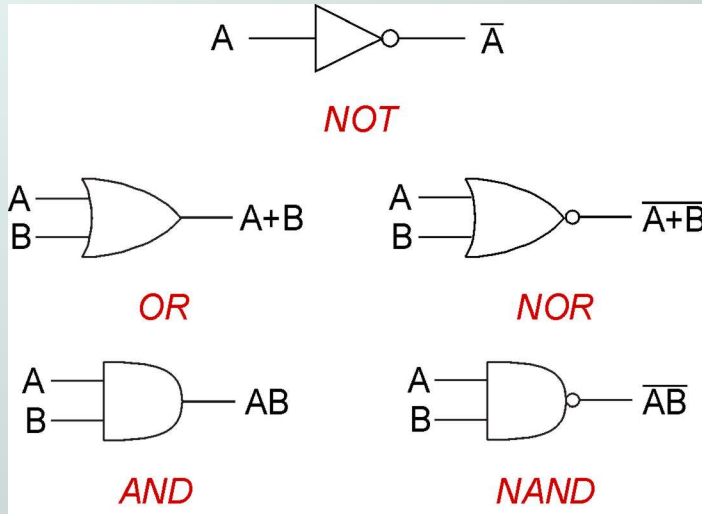
Series Parallel Circuits

- All transistors in an S-P circuit are of the same type (n or p)
- An SP circuit is constructed with the following rules
 - A wire is an SP circuit
 - A transistor is an SP circuit
 - Two or more SP circuits connected in **series** is an SP circuit
 - Two or more SP circuits connected in **parallel** is an SP circuit

Complement of an SP Circuit

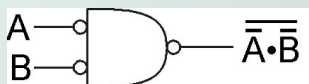
- Complement of an SP circuit consisting of a single transistor is the complementary type transistor (n becomes p and vice versa)
- To complement sub-circuits in series
 - Complement the sub-circuits
 - Connect them in parallel
- To complement sub-circuits in parallel
 - Complement the sub-circuits
 - Connect them in series
- Similar to De Morgan's Laws

Basic Logic Gates



DeMorgan's Law

- Converting AND to OR (with some help from NOT)
- Consider the following gate:



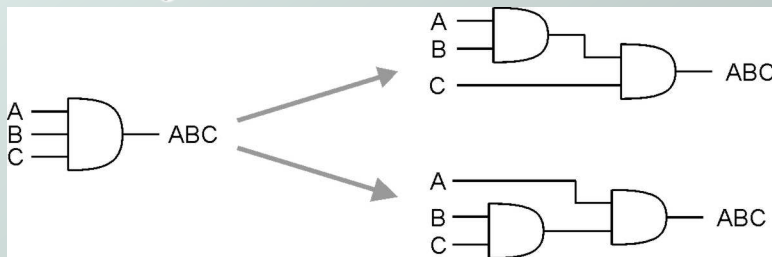
A	B	\bar{A}	\bar{B}	$\bar{A} \cdot \bar{B}$	$\overline{\bar{A} \cdot \bar{B}}$
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	0	1

Same as A OR B!

*To convert AND to OR
(or vice versa),
invert inputs and output.*

More than 2 Inputs?

- AND/OR can take any number of inputs.
 - AND = 1 if all inputs are 1.
 - OR = 1 if any input is 1.
 - Similar for NAND/NOR.
- Can implement with multiple two-input gates, or with single CMOS circuit.



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Summary

- MOS transistors are used as switches to implement logic functions.
 - n-type: connect to GND, turn on (1) to pull down to 0
 - p-type: connect to +2.9V, turn on (0) to pull up to 1
- Basic gates: NOT, NOR, NAND
 - Logic functions are usually expressed with AND, OR, and NOT
- DeMorgan's Law
 - Convert AND to OR (and vice versa) by inverting inputs and output

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Building Functions from Logic Gates

● **Combinational Logic Circuit**

- output depends only on the current inputs
- stateless

● **Sequential Logic Circuit**

- output depends on the sequence of inputs (past and present)
- stores information (state) from past inputs

● **We'll**

- first look at some useful combinational circuits,
- then show their limitations,
- and how to overcome them with sequential circuits

Announcement

Many students still have a zero on the paper and pencil Quiz0. Your score will not be entered until you see Sanjay during office hours. If you missed doing it, you can still earn full credit.

Print it off the schedule page, do it and see Sanjay during office hours (or make an appointment).

Deadline: Wednesday noon.