

Name: \_\_\_\_\_ Recitation Sec. \_\_\_\_\_ Date: \_\_\_\_\_

### CS270 Homework Assignment 3 (HW3)

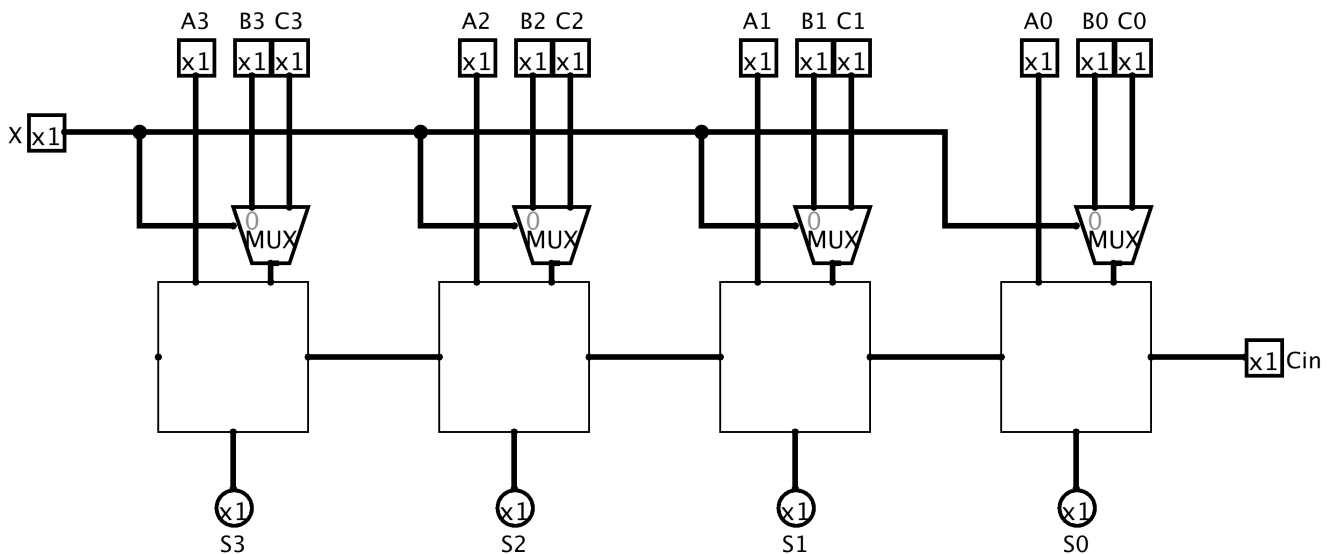
Due Thursday, October 3 (start of class)  
Homework and programming assignments are to be done individually.

#### Goals

To understand complex combinational circuits and sequential logic. This assignment requires the use of Logisim, the logic simulator that you have used for the previous assignment.

#### The Assignment

**Question 1 (30 points)** Consider the logic circuit below which is a 4-bit adder (each big square box is a full adder circuit, FA). Note how one of the inputs to each FA comes from a mux.



a. (5 points) What is the output of the circuit when X is 0 (describe in words)?

b. (5 points) What is it when X is 1?

c. (5 points) Describe succinctly what this circuit does, as a function of X?

**d. (15 points)** Using the above circuit as a building block (think of it as a box that takes three 4-bit words (A, B and C) and two 1-bit signals X and Cin, and produces a 4-bit output S and a Carry out), construct a circuit that implements a conditional adder/subtractor for two 4-bit numbers, P and Q, i.e., a circuit that will produce either P+Q or P-Q, depending on a control signal Z.

**Question 2 (25 points):** Consider Fig 3.21 (from textbook), the diagram of a 4-entry 3-bit memory.

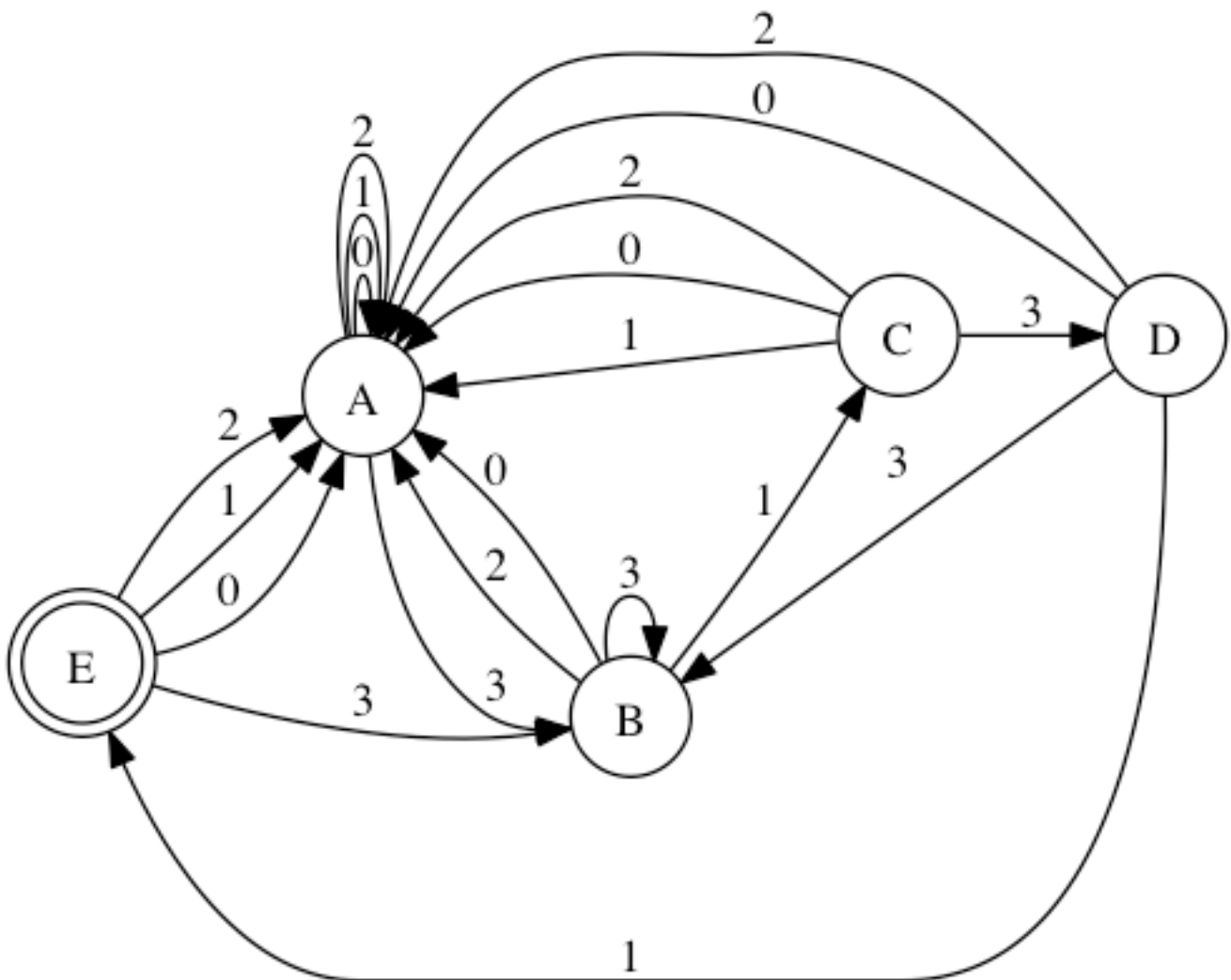
- a. (10 points)** Implement the circuit in Logisim and turn in the schematic (in a separate sheet).
- b. (2 points)** To read from the bottom-most memory location, what must be the values of A[1:0] and WE be?
- c. (2 points)** To change the number of entries from 4 to 50, how many address lines would be needed?
- d. (5 points)** Suppose that a certain register in the machine is to be used to address this new, 50-word memory. What is the number of bits that this register should have? How many additional locations can be added to this memory without changing the width of this register.
- e. (6 points)** Now we want to modify the memory so that at each of the 50 addresses, we can store a 16-bit value. How many bits are needed in the MAR? In the MDR? If we asked you to redraw the memory as in Fig 3.21, how many gated D-latches would you need?

**Question 3 (20 points):** We want to design a “pattern recognizer” sequential circuit. It takes two inputs  $I_1I_0$  that we view as a digit in radix-4. The machine produces an output 1 whenever the input pattern is 2323, but *overlaps* are allowed. For example the input sequence (the commas after every four characters are to improve readability, not part of the sequence) 2302,3232,3123,2301 will produce the output sequence 0000,0001,0100,0010,0. Note that these sequences are to be read left to right, and that the output is delayed one cycle after the input, so the first one output occurs *after* the 9<sup>th</sup> input at the 10<sup>th</sup> position.

- a. **(15 points)** Draw the state diagram of this finite state machine? Extra credit if you use the minimum number of states.

b. (5 points) How many states does this machine have? How many bits are required to represent the state of this machine?

Question 4 (25 points): Design and implement in Logisim, the state machine whose transition diagram is given below. Include both the circuit diagram as well as the truth table you used. Make sure your state machine outputs a “1” when it is in the acceptance state.



## **Submission Instructions**

All homework assignments will be handed in at the beginning of class on the due date. Logisim can save circuits as .gif pictures, please submit a picture for each circuit. After printing your circuits, you can cut and paste to this document, or attach to the back with a label showing the question number.

## **Late Policy**

Late assignments will be accepted up to 24 hours past the due date and time for a deduction of 25% and will not be accepted past this period. Late submissions should be made via email (.txt or .pdf files only), or by delivering the paper copy to my desk or under the door of room 256 in the Computer Science building.