Name: _____ Date: _____

CS270 Homework Assignment 2 (HW2)

Due Thursday, 9/15/2011 (start of class)
Homework and programming assignments are to be done individually.

Goals

To understand transistor basics, logic gates (NOT, NAND, NOR), DeMorgan's Law, decoders, multiplexers, and combinational logic. This assignment requires the use of a logic simulator called Logisim, which will be explained in class and practiced in the recitation. The Logisim web page, tutorial, and software is linked to from the class web page. To run the Logisim software, change to the directory containing the .jar file and type the following: **$ java -jar logisim-2.1.0.jar**

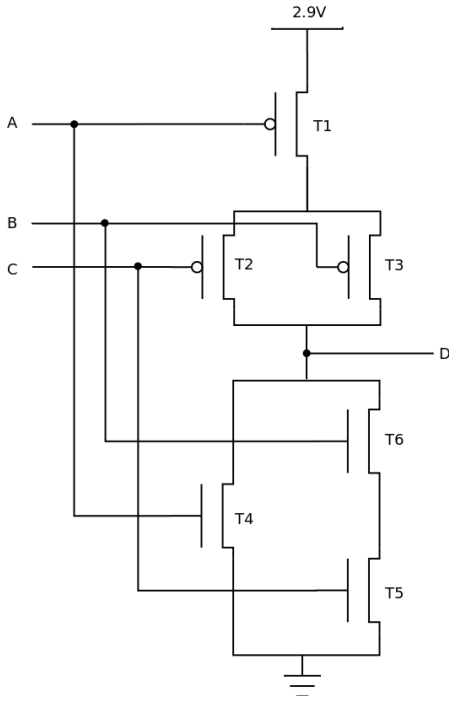
The Assignment

Question 1 (10 points): A transistor is a 3-terminal device where the voltage on the gate controls a "switch" between the drain and source. Fill in the table below that specifies the transistor state based on the type of the transistor (p-type or n-type) and the voltage at the controlling terminal (gate) with the words 'open' or 'closed'

Input	*p-type*	*n-type*
0 volts		
2.9 volts		

Question 2 (20 points): For the circuit below, fill in the table, as a function of the three input signals A, B and C, that describes the state of each of the transistors (open or closed). Based on that, fill out the last column -- the value of the output signal (D) that provides the truth table of the Boolean function that the circuit implements. Note that T1, T2, and T3 are p-type transistors, and T4, T5, and T6 are n-type.

What is the Boolean function that it implements? (Write answer below)



A	B	C	T1	T2	T3	T4	T5	T6	Out (V)
0	0	0							
0	0	1	closed				closed	open	
0	1	0							
0	1	1							
1	0	0		closed					
1	0	1							
1	1	0							
1	1	1							

1. Is there a simultaneous path from 2.9V to ground for any input combination?

2. Is there some input combination for which the output is “floating” (i.e., connected to neither of 2.9V or ground)?

3. Based on this, is this a well-designed circuit?

Question 3 (10 points):

Wikipedia describes De Morgan’s laws (http://en.wikipedia.org/wiki/De_Morgan%27s_laws):
In formal logic, De Morgan's laws are rules relating the logical operators "and" and "or" in terms of each other via negation, namely:

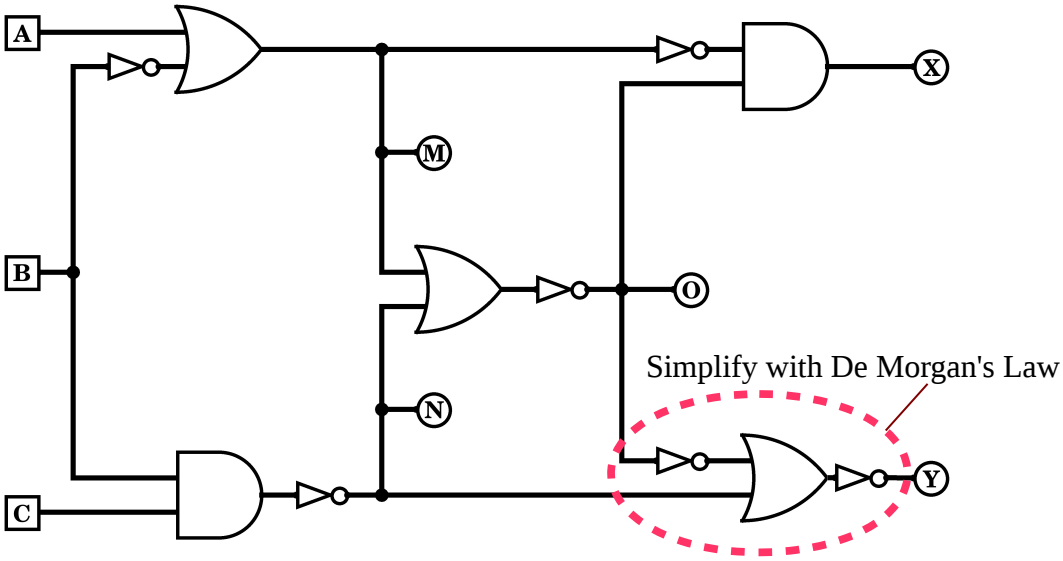
NOT (P OR Q) = (NOT P) AND (NOT Q)
NOT (P AND Q) = (NOT P) OR (NOT Q)

Fill in the truth table below that summarizes the first law shown above.

P	Q	P OR Q	NOT(P OR Q)	NOT P	NOT Q	(NOT P) AND (NOT Q)
0	0				1	
0	1	1				
1	0			0		
1	1					0

Question 4 (10 points): Design a 3-bit decoder using Logisim and turn in its schematic (on a separate sheet or in the space provided below).

Question 5 (25 points): Fill in the truth table for the following combinational circuit. The inputs are A, B, and C, and the outputs are M, N, O, X, and Y. Design the circuit in Logisim and turn in the schematic, making sure the truth table matches. Also, use De Morgan's law to simplify the highlighted part of the circuit that produces Y.



A	*B*	*C*	*M*	*N*	*O*	*X*	*Y*
0	*0*	*0*					
0	*0*	*1*		**1**			
0	*1*	*0*	**0**				**0**
0	*1*	*1*					
1	*0*	*0*			**0**		
1	*0*	*1*					
1	*1*	*0*					
1	*1*	*1*				**0**	

Question 6 (30 points): Design a combinational circuit for the following truth table. Inputs are A, B, and C, and the outputs are X and Y. Use the methodology described in Section 3.3.4 of the textbook, which employs successive arrays of AND and OR gates. Design the circuit in Logisim and turn in the schematic, making sure the truth table matches. Does this circuit resemble a decoder?

A	*B*	*C*	*X*	*Y*
0	*0*	*0*	**1**	**0**
0	*0*	*1*	**0**	**0**
0	*1*	*0*	**1**	**0**
0	*1*	*1*	**1**	**1**
1	*0*	*0*	**1**	**0**
1	*0*	*1*	**1**	**0**
1	*1*	*0*	**1**	**0**
1	*1*	*1*	**0**	**0**

Submission Instructions

All homework assignments must be handed in at the beginning of class on the due date. Logisim can save circuits as .gif pictures, please submit a picture for each circuit. After printing your circuits, you can cut and paste to this document, or attach to the back with a label showing the question number.

Late Policy

Late assignments will be accepted up to 48 hours past the due date and time. There will be a penalty of 10% for each delay by 24 hours. Assignments will not be accepted past the 48 hour delay. Late submissions must be made via RamCT.