Schedule : Fall 2019

This is the tentative schedule of Mélange group for the Fall 2019 semester.
Meeting time & Place : Wednesdays 10:00 AM - 11:00 AM @ CSB 305

WEEK	DATE	TOPIC	PRESENTER
0	08/28/2019	Intros and Planning	all
1	09/04/2019	Canceled	-
2	09/11/2019	Research work	Sanjay Rajopadhye
3	09/18/2019	Research work	Louis-Noël Pouchet
4	09/25/2019	Effective Resource Management for Enhancing Performance of 2D and 3D Stencils on GPUs	Louis-Noël Pouchet
5	10/02/2019	Understanding Reuse, Performance, and Hardware Cost of DNN Dataflows: A Data-Centric Approach	Sanjay Rajopadhye
6	10/09/2019	A Framework for Enhancing Data Reusevia Associative Reordering	Louis-Noël Pouchet
7	10/16/2019	Canceled	-
8	10/23/2019	Canceled	-
9	10/30/2019	Program Equivalence Analysis Using Machine Learning	Steve Kommrusch
10	11/06/2019	Playing with number representations for energy efficiency: An Introduction to Approximate Computing	Olivier Sentieys
11	11/13/2019	Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks	Brandon Gildemaster
12	11/20/2019	Pruning and acceleration of Deep Neural Networks	Janarthanan Sarma
13	11/27/2019	Fall Break	
14	12/04/2019	The Next 700 Accelerated Layers: From Mathematical Expressions of Network Computation Graphs to Accelerated GPU Kernels, Automatically	Louis Narmour
15	12/06/2019	Generating piecewise-regular code from irregular structures	Travis Augustine
16	12/11/2019		
17	12/18/2019	Exam week	

Current Reading Pool

- Nicolas Vasilache, Oleksandr Zinenko, Theodoros Theodoridis, Priya Goyal, Zachary Devito, William S. Moses, Sven Verdoolaege, Andrew Adams, Albert Cohen, The Next 700 Accelerated Layers: From Mathematical Expressions of Network Computation Graphs to Accelerated GPU Kernels, Automatically, ACM Trans. Archit. Code Optim. 2019
- Travis Augustine, Janarthanan Sarma, Louis-Noël Pouchet, Gabriel Rodríguez, Generating Piecewise-regular Code from Irregular Structures, PLDI 2019
- Hyoukjun Kwon, Michael Pellauer, Tushar Krishna, Understanding Reuse, Performance, and Hardware Cost of DNN Dataflows: A Data-Centric Approach, CoRR 2018
- Y. H. Chen, T. Krishna, J. S. Emer, V. Sze, Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks, IEEE Journal of Solid-State Circuits 2017

- Prashant Singh Rawat, Changwan Hong, Mahesh Ravishankar, Vinod Grover, Louis-Noël Pouchet, P. Sadayappan, Effective Resource Management for Enhancing Performance of 2D and 3D Stencils on GPUs, GPGPU '16
- Kevin Stock, Martin Kong, Tobias Grosser, Louis-Noël Pouchet, Fabrice Rastello, J. Ramanujam, P. Sadayappan, A Framework for Enhancing Data Reuse via Associative Reordering, PLDI '14

Previous Reading Pool

- Y. H. Chen, T. Krishna, J. S. Emer, V. Sze, Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks, IEEE Journal of Solid-State Circuits 2017
- Chris Cummins, Pavlos Petoumenos, Zheng Wang, Hugh Leather, Synthesizing benchmarks for predictive modeling
- Johannes Doerfert, Tobias Grosser, Sebastian Hack, Optimistic Loop Optimization
- William F. Ogilvie, Pavlos Petoumenos, Zheng Wang, Hugh Leather, Minimizing the Cost of Iterative Compilation with Active Learning, CGO '17
- Wlodzimierz Bielecki, Marek Pa lkowski, Tiling Arbitrarily Nested Loops by Means of the Transitive, Int. J. Appl. Math. Comput. Sci. 2016
- Wenlei Bao, Changwan Hong, Sudheer Chunduri, Sriram Krishnamoorthy, Louis-Noel Pouchet, Fabrice Rastello, P. Sadayappan, Static and Dynamic Frequency Scaling on Multicore CPUs, ACM Trans. Archit. Code Optim. 2016
- U. Bondhugula, V. Bandishti, I. Pananilath, Diamond Tiling: Tiling Techniques to Maximize Parallelism for Stencil Computations, IEEE Transactions on Parallel and Distributed Systems 2016
- Audrunas Gruslys, R{ '{e}}mi Munos, Ivo Danihelka, Marc Lanctot, Alex Graves, Memory-Efficient Backpropagation Through Time, CoRR 2016
- Daniel J. Milroy, Allison H. Baker, Dorit M. Hammerling, John M. Dennis, Sheri A. Mickelson, Elizabeth R. Jessup, Towards Characterizing the Variability of Statistically Consistent Community Earth System Model Simulations, Procedia Computer Science 2016
- T. Nowatzki, J. Menon, C. H. Ho, K. Sankaralingam, Architectural Simulators Considered Harmful, IEEE Micro 2015
- J. D. Garvey, T. S. Abdelrahman, Automatic Performance Tuning of Stencil Computations on GPUs, 2015 44th International Conference on Parallel Processing
- Eric Chung Kalin Ovtcharov, Accelerating Deep Convolutional Neural Networks Using Specialized Hardware
- Protonu Basu, Mary Hall, Samuel Williams, Brian Van Straalen, Leonid Oliker, Phillip Colella, Compiler-Directed Transformation for Higher-Order Stencils, IPDPS '15
- Sharan Chetlur, Cliff Woolley, Philippe Vandermersch, Jonathan Cohen, John Tran, Bryan Catanzaro, Evan Shelhamer, cuDNN: Efficient Primitives for Deep Learning, CoRR 2014
- Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John

Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger, A Reconfigurable Fabric for Accelerating Large-scale Datacenter Services, ISCA '14

- Martin Kong, Richard Veras, Kevin Stock, Franz Franchetti, Louis-No “{e}l Pouchet, P. Sadayappan, When Polyhedral Transformations Meet SIMD Code Generation, SIGPLAN Not. 2013
- Louis-Noel Pouchet, Peng Zhang, P. Sadayappan, Jason Cong, Polyhedral-based Data Reuse Optimization for Configurable Computing, FPGA '13
- Sven Verdoolaege, Gerda Janssens, Maurice Bruynooghe, Equivalence Checking of Static Affine Programs Using Widening to Handle Recurrences, ACM Trans. Program. Lang. Syst. 2012
- Vinayaka Bandishti, Irshad Pananilath, Uday Bondhugula, Tiling Stencil Computations to Maximize Parallelism, SC '12
- Henry Wong, Vaughn Betz, Jonathan Rose, Comparing FPGA vs. Custom Cmos and the Impact on Processor Microarchitecture, FPGA '11
- M.-W. Benabderrahmane, L.-N. Pouchet, Cohen A., C. Bastoul, The Polyhedral Model Is More Widely Applicable Than You Think, LNCS
- Vasily Volkov, James W. Demmel, Benchmarking GPUs to Tune Dense Linear Algebra, SC '08
- Andrew R. Putnam, Dave Bennett, Eric Dellinger, Jeff Mason, Prasanna Sundararajan, CHiMPS: A High-level Compilation Flow for Hybrid CPU-FPGA Architectures, FPGA '08
- Milind Kulkarni, Keshav Pingali, Bruce Walter, Ganesh Ramanarayanan, Kavita Bala, L. Paul Chew, Optimistic Parallelism Requires Abstractions, PLDI '07
- Paul Feautrier, Scalable and Structured Scheduling, Int. J. Parallel Program. 2006
- Steven J. Deitz, Bradford L. Chamberlain, Lawrence Snyder, Eliminating Redundancies in Sum-of-product Array Computations, ICS '01
- Martin Griebl, Paul Feautrier, Christian Lengauer, Index Set Splitting, International Journal of Parallel Programming 2000
- J-F. Collard, D. Barthou, P. Feautrier, Fuzzy Array Data Flow Analysis, Journal of Parallel and Distributed Computing 1997
- J. Cong, Yuzheng Ding, FlowMap: an optimal technology mapping algorithm for delay optimization in lookup-table based FPGA designs, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
- Paul Feautrier, Some Efficient Solutions to the Affine Scheduling Problem {Part I}. One-dimensional Time, International Journal of Parallel Programming 1992
- Paul Feautrier, Some Efficient Solutions to the Affine Scheduling Problem {Part II}. Multidimensional Time, International Journal of Parallel Programming 1992
- P. Feautrier, Dataflow analysis of array and scalar references, International Journal of Parallel Programming 1991
- Patrice Quinton, Vincent van Dongen, The mapping of linear recurrence equations on regular arrays, Journal of VLSI signal processing systems for signal, image and video technology 1989

- D. Baxter, R. Mirchandaney, J. H. Saltz, Run-time Parallelization and Scheduling of Loops, SPAA '89
- F. Irigoin, R. Triolet, Supernode Partitioning, POPL '88
- Sanjay V. Rajopadhye, S. Purushothaman, Richard Fujimoto, On Synthesizing Systolic Arrays from Recurrence Equations with Linear Dependencies, Proceedings of the Sixth Conference on Foundations of Software Technology and Theoretical Computer Science