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Pass-transistor logic design

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Logic functions implemented using CMOS transmission gates provide a moderate improvement in area and speed over logic gate implementations. Several techniques for the implementation of pass transistor logic are presented. These techniques use only nMOS transistors in the pass network. The output logic level is restored using additional circuitry. The proposed designs require less silicon area, less power dissipation, and operate at higher speeds compared with the conventional CMOS pass-transistor networks. The speed of operation depends mainly on the circuitry used to restore the output signal of the pass network. The different techniques are compared with respect to the layout area and operating speed.

1. Introduction

Pass-transistor network realizations of logic functions in general result in area savings and higher operating speed when compared with the corresponding gate logic realizations. Moreover, pass-transistor networks can be synthesized automatically by using formal design procedures (Radhakrishnan *et al.* 1985). In pass-transistor logic, the pass device is used as a switch to connect two nodes together conditionally, and is often appropriate when the logic function is conveniently conceptualized as signals or tokens being conditionally steered through a network (Glasser and Dobberpul 1985).

NMOS pass-transistor logic using the nMOS transistor as a pass element has shown substantial area savings, speed improvements, and less power dissipation compared to gate logic implementations. Systematically designed nMOS pass-transistor networks can reduce complex functions to highly regular structures that operate faster than conventional nMOS logic gates (Whitaker 1983). These nMOS pass-transistor networks, however, have poor low-to-high transition characteristics. CMOS transmission gates overcome this disadvantage by using a parallel combination of pMOS and nMOS transistors. As a result, however, the conventional CMOS pass transistor logic provides only a moderate area and speed improvement when compared to CMOS gate logic (Pasternak *et al.* 1985).

This paper presents several techniques for implementing logic functions using pass-transistors. The output of an nMOS pass network is restored to achieve the maximum voltage swing at the output node, as well as low rise and fall times. The objective is to achieve low area, high speed of operation, and low power dissipation. The different techniques presented are compared with traditional pass-transistor logic designs with respect to the transition delays, the area and the

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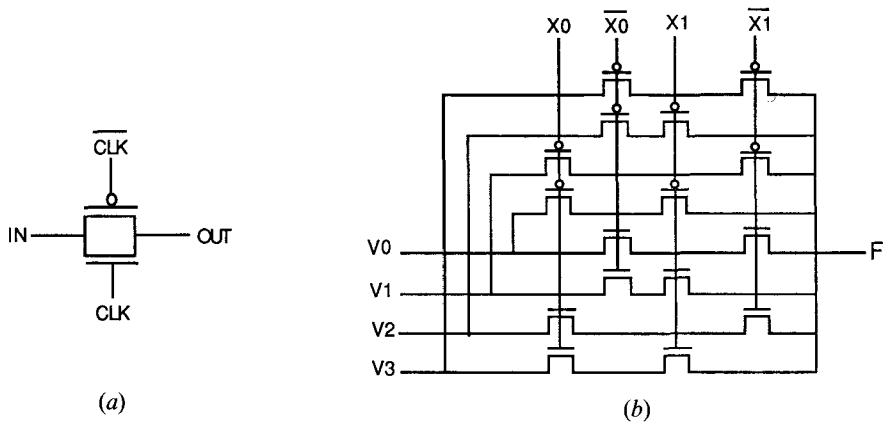


Figure 1. Conventional CMOS pass-transistor logic: (*a*) CMOS transmission gate, and (*b*) 4-to-1 multiplexer implementation.

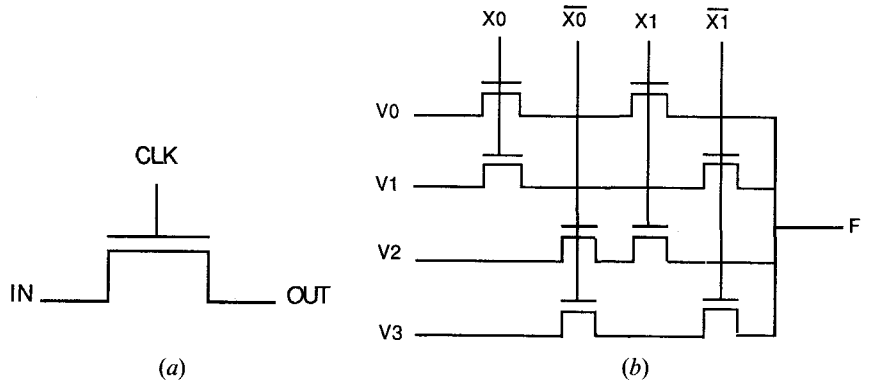


Figure 2. NMOS pass-transistor logic: (*a*) NMOS pass-transistor, and (*b*) 4-to-1 multiplexer implementations.

power dissipation. In the next section, the existing pass-transistor logic implementations are reviewed. Differential buffers or sense amplifiers can be used to restore the output logic level of a simple pass-transistor network. This technique is described in §3. Section 4 presents several alternative pass-transistor logic design techniques that have good rise and fall characteristics as well as low area. Different design techniques are compared in §5.

2. NMOS, CMOS and differential pass-transistor logic

The CMOS transmission gate shown in Fig. 1(*a*), is the basic element used in conventional CMOS pass-transistor logic designs. The signal flow through the gate is controlled by complementary clock signals. The pMOS transistor passes logic '1' without degradation, while the nMOS transistor passes logic '0' without degradation; hence the output signal is a good replica of the input signal, and the gate delay time between the input and the output is almost independent of the input

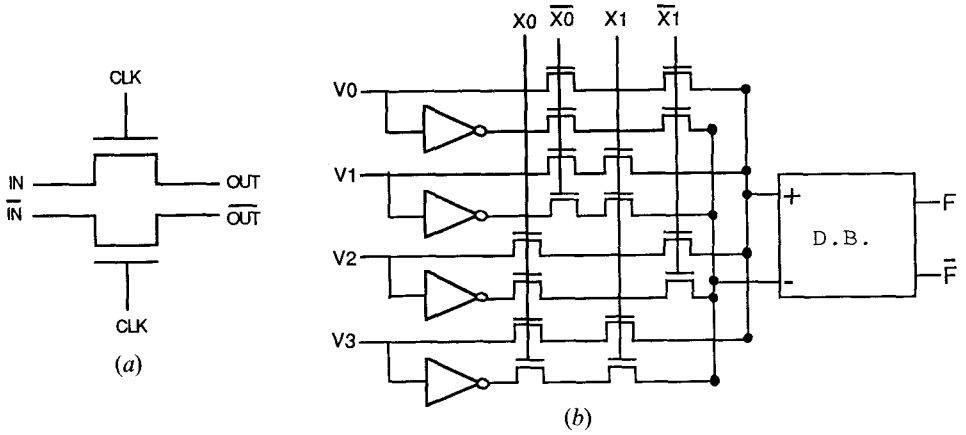


Figure 3. Differential pass-transistor logic (DPTL): (*a*) differential pass element, and (*b*) 4-to-1 multiplexer implementations.

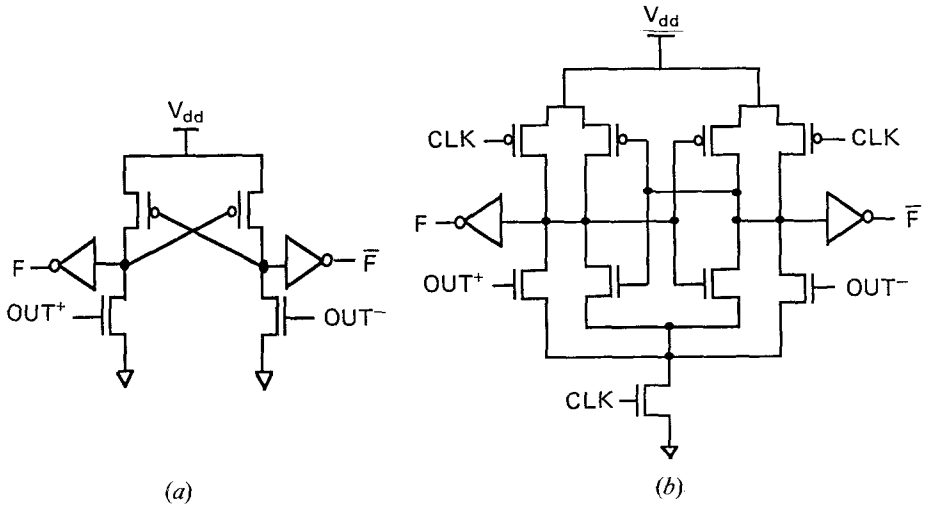


Figure 4. Differential buffers: (*a*) static, and (*b*) clocked.

signal voltage level (Annaratone 1985, Elmasry 1985). Figure 1(*b*) shows the conventional CMOS pass-transistor implementation of a 4-to-1 multiplexer. The nMOS pass-transistor logic uses only an nMOS transistor as the pass element as shown in Fig. 2(*a*). This gate passes logic '0' efficiently but not logic '1', and the gate delay is dependent on the input signal. The nMOS pass-transistor implementation of the 4-to-1 multiplexer is shown in Fig. 2(*b*).

In the CMOS version, both p and n diffusions are used in the layout, thus doubling the number of transistors. Parameters extracted from layouts of both nMOS and CMOS pass networks show that the output capacitance of the nMOS pass network is about half that of the CMOS pass network. This causes the circuit to be inherently slow. Use of both p and n channel transistors result in substantial n-plane to p-plane interconnects, and the required well-to-device spacing reduces the area efficiency (Pasternak *et al.* 1985). Eliminating the pMOS transistors

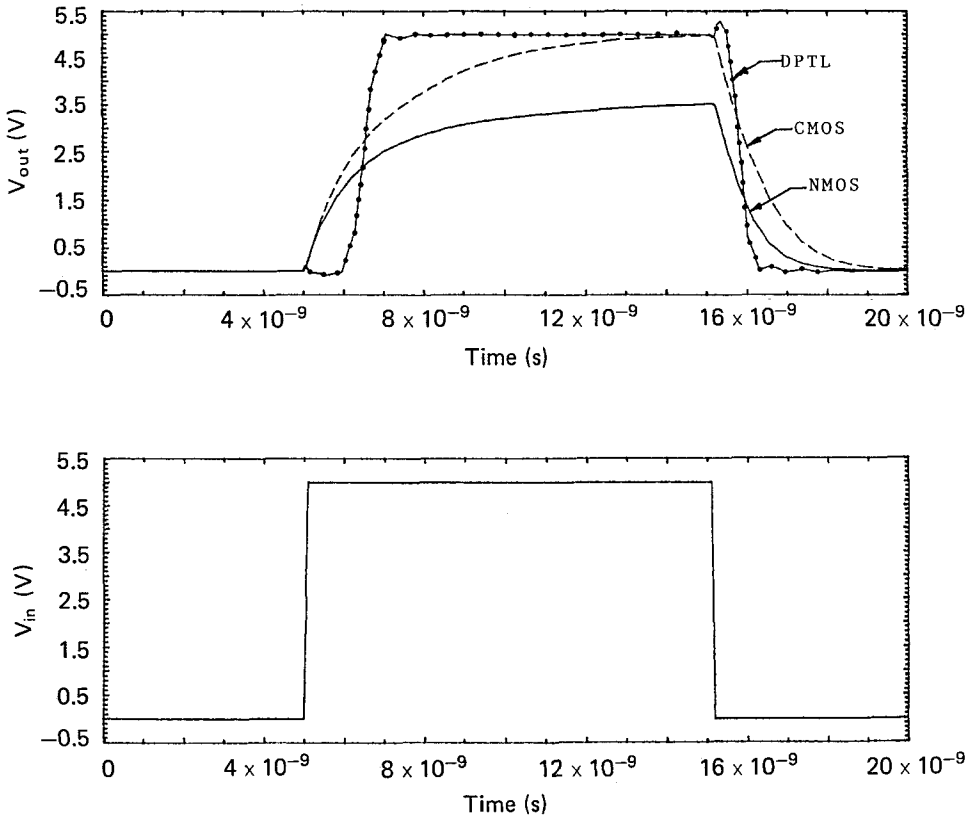


Figure 5. Comparison of CMOS-PTL, NMOS-PTL, and DPTL using SPICE (—— for NMOS-PTL; ---- for CMOS-PTL; –·–·– for DPTL).

results in a substantial area saving in the nMOS version. The maximum output voltage of the nMOS pass network, however, is $(V_{dd}-V_{th})$ where V_{th} is the threshold voltage of the nMOS transistor and V_{dd} is the power supply voltage. This poses several problems including reduced noise margins and the inability of a pass network output to drive the gate of another pass transistor. The nMOS and CMOS implementations are compared in Table 1.

The differential pass-transistor logic (DPTL), is a technique which overcomes the problems of conventional CMOS pass networks (Pasternak *et al.* 1985). In this technique, the CMOS transmission gate is replaced by the differential pass element shown in Fig. 3(*a*). Figure 3(*b*) shows the DPTL implementation of a 4-to-1 multiplexer. The input signal is differentiated, passed to the output, and a differential buffer is used to restore the differential output signal to 0 and V_{dd}, respectively, for logic levels '0' and '1'. This technique offers greater area efficiency and higher speed of operation than the conventional CMOS pass-transistor logic implementation (Pasternak *et al.* 1985).

In DPTL, a differential amplifier is used to generate the output voltage. Two forms of differential buffers have been proposed (Pasternak *et al.* 1985): a static differential buffer and a clocked differential buffer, as shown in Fig. 4. The static

differential buffer shown in Fig. 4(*a*) is simply a cascade voltage switch inverter. The cross-coupled p pull-up transistors counteract the effect of charge leakage at the drain of the pull-down. Positive feedback applied to the p pull-ups causes the gate to switch, so that nodes F and $\bar{F}$ are pulled high or low, when either input is low (0 V) and the other is higher than V_{th} (Annaratone 1985, Weste 1985). The rise time of the output signal at node F is associated with the input signal at node OUT^+, while its fall time is associated with the input signal at input OUT^-.

The clocked differential buffer shown in Fig. 4(*b*) is basically a RAM sense amplifier (Pasternak *et al.* 1985, Annaratone 1985). The cross-coupled inverters enhance the data storage ability at low frequencies and reduce charge sharing during the pull-down period. This circuit has the advantages of dynamic logic, and therefore offers fast logic transition whenever one of the inputs is low (0 V), and the other is higher than V_{th} before the clock is applied.

Figure 5 shows the output characteristics, obtained using SPICE, for the 4-to-1 multiplexer implemented using nMOS pass-transistor logic, CMOS pass-transistor logic, and DPTL with a clocked differential buffer. The DPTL offers a significantly lower delay than the other two circuits. However, it requires more elements than the corresponding nMOS implementation. DPTL implementation requires 16 transistors for the pass network, 4 inverters and 13 transistors for the differential buffer for a total of 37 transistors, while the nMOS pass-transistor implementation requires only 8 transistors (and one inverter if differential output is required). The nMOS pass network offers area saving and less power dissipation compared to the DPTL implementation, but provides a poor low-to-high transition. In the next section, we show how the output of nMOS pass networks can be restored to achieve performance better than DPTL, but with much less hardware.

3. Differential buffers and sense amplifiers

DPTL uses inverters at the inputs to the pass network, and propagates both the signal and its complement to the output. This results in more than doubling the area required by the pass network. However, since the n-network passes '0' logic efficiently, either the signal or its complement, whichever is zero, is passed to the output before the other. This is sensed by a differential buffer, which generates the correct output voltage. In this section, we show that a performance similar to DPTL can be achieved by using a simple nMOS pass network with a sensing circuit at the output. This results in a significant saving in area.

Rather than passing both the pass variable and its complement through separate pass networks, we propose the use of a single pass network with the output signal restored using a restoring circuit. The differential buffer requires two complementary inputs, hence the output signal of the nMOS pass network has to be differentiated using an inverter as shown in Fig. 6. However, the output rise time can be improved by introducing another inverter before the OUT^+ node. SPICE simulation results for both an nMOS pass network with differential buffers and DPTL with identical restoring circuits are shown in Fig. 7. It is seen that the nMOS pass-transistor network followed by the differential buffer provides a higher speed of operation while requiring significantly less area than DPTL.

The static differential buffer can be modified to a clocked version as shown in Fig. 8(*a*). This version offers faster switching than the static version, therefore only

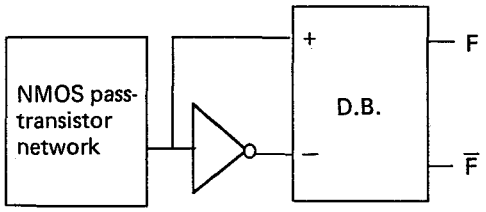


Figure 6. NMOS pass network with differential buffer.

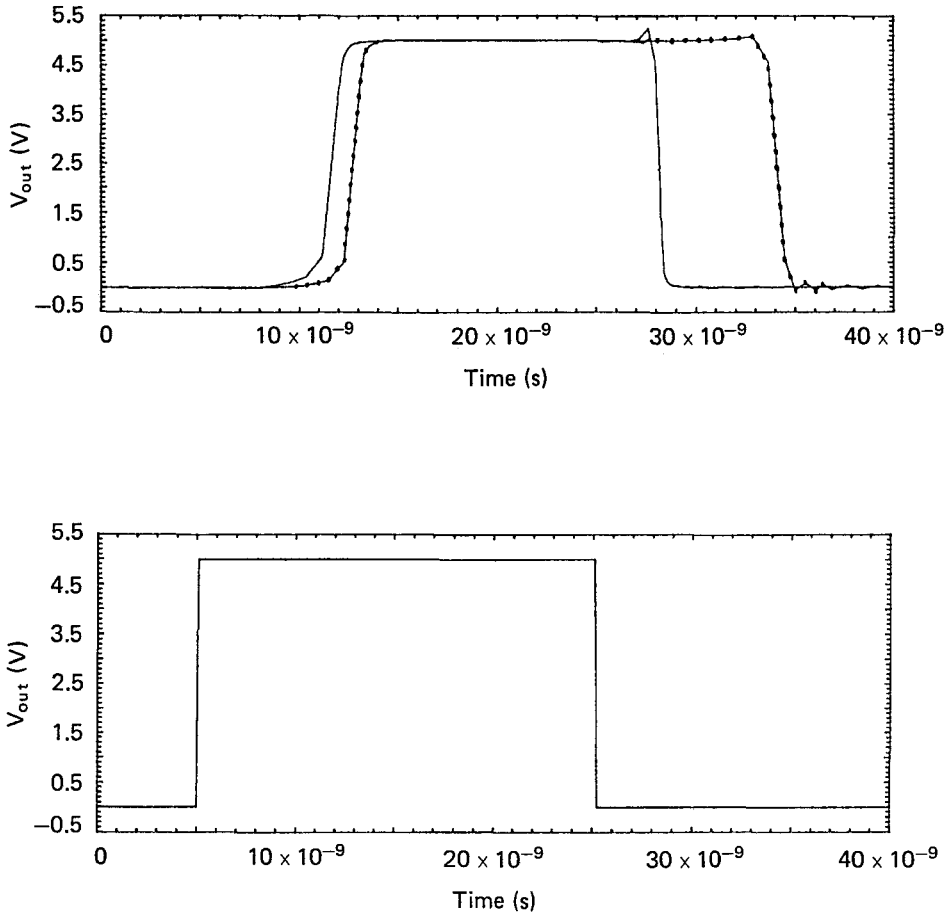


Figure 7. Simulation results for circuits using static buffers (—— for NMOS pass network; –·–·– for DPTL).

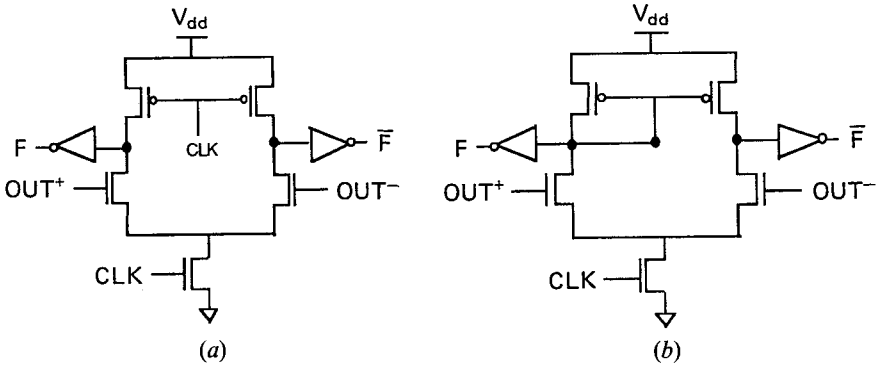


Figure 8. Alternative differential buffer versions.

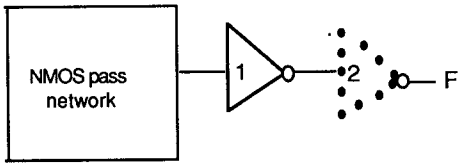


Figure 9. NMOS pass network with two buffers.

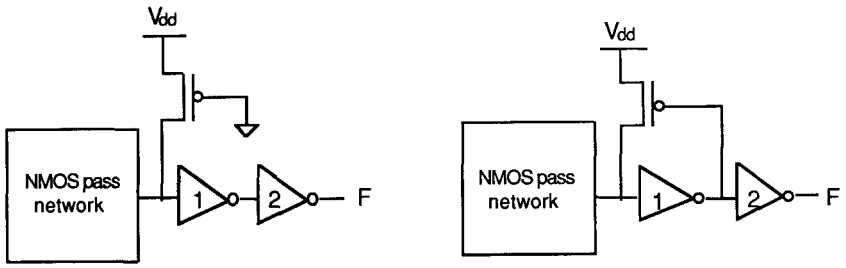
one inverter is used to differentiate the output signal of the nMOS pass network. The sense amplifier shown in Fig. 8(*b*) can also be used as a restoring circuit. This circuit senses a small difference between input levels OUT^+ and OUT^-, and amplifies this difference to provide a fast transition to either V_{dd} or to V_{ss}(gnd) (Pasternak *et al.* 1985). We compare the performance and the area of these proposed designs with DPTL in §5.

4. Alternative pass-transistor logic implementations

In this section, we present several techniques that can be used to restore the output signal of a pass-transistor network to V_{dd} and V_{ss}(gnd) for logic '0' and '1'. All the circuits described below use CMOS technology. However, there are nMOS counterparts for these circuits that can be used with nMOS.

4.1. *Use of restoring buffers*

A simple way to restore the output signal of an nMOS pass network to normal logic levels is to use two inverters (buffers) as shown in Fig. 9. A buffer can be either a CMOS inverter or a pseudo nMOS inverter. Two CMOS inverters having a switching threshold voltage of $V_{dd}/2$ may be used. Since the nMOS pass network has a poor output low-to-high transition and a good high-to-low transition, an improvement in speed of operation can be achieved by modifying the first inverter to have a switching threshold voltage less than $V_{dd}/2$ without affecting the size of the layout. For example, when $V_{dd}=5$ V, the first inverter can be modified so that its switching threshold voltage is 1·8 V instead of 2·5 V.



(*a*) (*b*)

Figure 10. NMOS pass network with a pMOS pull-up transistor: (*a*) pseudo nMOS version, and (*b*) latched version.

4.2. *Use of pull-up transistors*

A p-pull up transistor can be used at the output of a pass network to improve, the low-to-high transition. In this case, the current through the pull-up transistor will restore the output voltage for logic level '1' to V_{dd}. In the case of high-to-low transition, however, the pass network has to sink the current through the pull-up transistor in addition to discharging the capacitance of the output node. The p pull-up transistor must be weak, i.e. the W/L ratio has to be low in order to maintain a low fall time of the output. Two inverters can be used as shown in Fig. 10(*a*) to achieve equal rise and fall times and to provide current driving capability. Owing to the current through the pull-up transistor, this version will dissipate power when the output voltage is low.

An alternative is to connect the gate of the pull-up transistor to the output of the first buffer as shown in Fig. 10(*b*). In this case, when the output of the pass network exceeds the switching threshold of the inverter, the pull-up transistor is turned on, thus aiding the low-to-high transition of the pass network output. In this case, the performance can be further improved by changing the switching threshold voltage of the first inverter to a value below $V_{dd}/2$. The implementation used in this study, for example, has an inverter switching threshold of $0{\cdot}36\,V_{dd}$, and $W/L = 0{\cdot}5$ for the p pull-up transistor.

5. Results

This paper has presented several pass-transistor logic designs that overcome the disadvantages associated with traditional pass-transistor circuit designs. A 4-to-1 multiplexer circuit has been used as an example to compare the different design techniques. The circuits have been layed out using MOSIS 3 micron design rules for CMOS p-well technology. The circuit parameters were extracted using the MEXTRA circuit extractor, and the circuit level simulations used SPICE. A summary of results is provided in Tables 1–4, which list the low-to-high and high-to-low transition delays, rise and fall times, the area occupied by each design, and the power dissipation of each circuit for a 10 MHz input pattern. The transition delay is the time interval between the points in the input and output waveforms at which the voltage is $0{\cdot}5\,V_{dd}$. The results for nMOS and CMOS pass-transistor implementations are presented in Table 1. While the nMOS pass network has the lowest area, it has a poor low-to-high transition and a logic '1' voltage of

	nMOS	CMOS
Rise time (ns)	>15	5·0
Fall time (ns)	2·0	3·5
Transition delay		
low-to-high (ns)	2·0	1·2
high-to-low (ns)	0·5	1·0
Area (μm^2)	58 × 54	103 × 76

Table 1. Characteristics of NMOS and CMOS pass-transistor implementations of a 4-to-1 multiplexer.

Restoring circuit	Static diff. buffer	Clocked buffer	Clocked static buffer	Sense amplifier
Rise time (ns)	8·0	2·0	2·0	1·8
Fall time (ns)	10·0	1·8	2·2	5
Transition delay				
low-to-high (ns)	8·0	1·5	1·5	1·3
high-to-low (ns)	9·0	1·5	1·8	2·0
Area (μm^2)	180 × 281	180 × 343	180 × 312	180 × 312
Power dissipation (μW)	237·5	86·7	580·9	68·2

Table 2. Characteristics of differential pass-transistor implementation of a 4-to-1 Mux, with a static differential buffer, a clocked buffer, a clocked static buffer and a sense amplifier, respectively, to restore the output.

Restoring circuit	Static diff. buffer	Clocked buffer	Clocked static buffer	Sense amplifier
Rise time (ns)	5·2	2·0	2·0	1·9
Fall time (ns)	4·0	1·5	0·9	0·8
Transition delay				
low-to-high (ns)	5·0	1·5	1·5	1·4
high-to-low (ns)	3·8	1·2	0·8	1·0
Area (μm^2)	64 × 179	88 × 216	64 × 179	75 × 156
Power dissipation (μW)	162	49	33	49

Table 3. Characteristics of the implementation of a 4-to-1 Mux, by restoring the output of an nMOS pass-transistor network with a static buffer, a clocked buffer, a static clocked buffer and a sense amplifier, respectively.

($V_{dd} - V_{th}$). Although this problem is overcome in CMOS by using a transmission gate as the pass element, CMOS suffers from lower speed and a higher area requirement.

Differential pass-transistor logic designs proposed by Pasternak *et al.* (1985) achieve high speed (low transition delays) and full logic swing. They use a static differential buffer or a clocked differential buffer for restoring the output of the differential pass-transistor network. Table 2 summarizes the results for these two circuits as well as two new differential pass-transistor implementations with a sense amplifier and a clocked static differential buffer as the restoring circuit. Comparison of Tables 1 and 2 show that DPTL does offer significant improvement in

	Modified CMOS	Pseudo nMOS	Latched buffers
Rise time (ns)	2·0	1·8	2·6
Fall time (ns)	2·0	2·6	2·5
Transition delay			
low-to-high (ns)	1·8	1·7	2·5
high-to-low (ns)	1·5	2·4	2·7
Area (μm^2)	58 × 102	58 × 118	58 × 118
Power dissipation (μW)	41·6	2796	577

Table 4. Characteristics of an implementation of a 4-to-1 Mux using modified buffers (Fig. 6(*b*)), a pseudo nMOS restoring circuit (Fig. 10(*a*)) and latched buffers (Fig. 10(*b*)), respectively, to restore the output of an nMOS pass-transistor network.

performance, but at a significant cost in terms of area. If the DPTL configuration is used, a clocked static differential buffer or a sense amplifier (Fig. 8) provides a delay comparable to that of the restoring circuit proposed by Pasternak *et al.* (1985) without significantly affecting other parameters.

Whenever a differential pass transistor circuit is used (with either a static differential buffer or a clocked differential buffer as proposed by Pasternak *et al.* (1985), or with a sense amplifier or a static clocked buffer as proposed in §3), the circuit area becomes significantly larger than that in normal CMOS or nMOS pass-transistor logic designs. Table 3 shows the results when a simple nMOS pass transistor network is used, with a restoring circuit at the output. Comparison of Table 2 and Table 3 shows that the output restoring circuit used with an nMOS pass network instead of a differential pass-transistor network, results not only in a significant reduction in area, but also an increase in speed. The configuration shown in Fig. 6 is always faster compared to the DPTL circuit using the same restoring circuit. The saving in area is due to the fact that a pass-transistor network uses less than half the number of transistors used in a differential pass-transistor circuit. The improvement in delay can be attributed to the corresponding decrease in the output capacitance of the circuit. For the 4-to-1 multiplexer, for example, the DPTL circuit with static differential buffer requires 32 transistors, while the nMOS pass network with the same buffer requires only 16 transistors. The latter also has much faster rise and fall characteristics.

Table 4 lists the results for the pass-transistor circuit designs proposed in §4. These design techniques have been presented to achieve low delay and low area compared to traditional pass-transistor logic designs. They include the use of simple inverters, inverters with pull-up transistors and inverters with pull-up transistors connected to form a latch. Each of these circuits require a significantly lower area compared to the circuits using differential buffers or sense amplifiers, but have a slightly higher delay. They overcome all the disadvantages of traditional nMOS, CMOS and differential pass-transistor logic designs with very little overhead.

6. Conclusions

Several pass transistor logic implementations have been presented that require significantly less area than conventional CMOS and differential pass-transistor

logic designs, but have better performance characteristics. The improvements have been achieved by the use of a restoring circuit at the output of a simple pass-transistor network.

Acknowledgments

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