Optimal Clustering and Statistical Identification of Defective ICs using I_{DDQ} Testing

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Abstract

Instead of relying on setting an arbitrary threshold current value as in traditional IDDQ testing, clustering based test technique relies on the characteristics of an IC with respect to all the other ICs in a lot to make a test decision. An improvement in the cluster analysis technique for I_{DDQ} testing is presented. Results of applying this technique to data collected on a high volume graphics chip are presented. The results are also compared against a newer more innovative form of I_{DDQ} testing.

1. Introduction

Historically I_{DDQ} testing has been used in addition to the functional tests to improve the quality of the device under test (DUT) [1, 2]. While I_{DDQ} testing contributes significantly to the thoroughness of the test strategy, there has been reluctance on the part of IC foundries to adopt I_{DDQ} testing as part of their overall test strategy for several reasons. Traditional I_{DDQ} testing involves in setting an arbitrary threshold quiescent current and classifying ICs as good or bad (test decision) based on this threshold current value.

While this approach seems intuitively sound, it suffers from three primary drawbacks; there is no commonly accepted procedure to set these threshold current values [3]. There is an underlying assumption that the quiescent current levels of a defective IC will be significantly higher than the quiescent current levels of a good IC and finally there is no procedure to distinguish between the elevated quiescent current levels caused by a defect and the elevated quiescent current levels that are an attribute of normal circuit operation. The assumption that there will be a significant difference in the good and defective quiescent current levels will no longer be valid in the future [4]. The die geometries have continued to shrink with advances in process technologies, leading to new design techniques like SOC (System On Chip). This increases the complexity and the amount of logic on an IC substantially, which in turn increases the quiescent current levels even on a good IC. Since an underlying principle of I_{DDQ} testing

is the ability to distinguish between the good and defective current levels and as the difference between good quiescent current levels and defective levels becomes progressively smaller leading to a difficulty in making a test decision, the notion that I_{DDQ} testing is reaching its limits is of concern.

This concern has led to newer and more innovative approaches to I_{DDQ} testing. The two primary approaches are Current Signatures [5, 6] and ΔI_{DDQ} Testing [7, 8]. In the production testing of both these approaches, instead of setting an arbitrary threshold for the quiescent currents, the quiescent currents are measured over a range of test vectors and the measured current values for each test vector are compared with the current values measured for the previous test vector. Any IC that displays a significant difference in the measured currents for any two successive test vectors is classified as defective. While both these approaches partly solve some of the issues involved with traditional I_{DDQ} testing specifically the problems involved in setting an arbitrary threshold value for quiescent current levels, there are still some drawbacks. With the increased complexity of the ICs, among the test vectors applied there might be some test vectors that produce high quiescent currents even in good devices. Thus instead of being considered a design trait, a normal circuit operation that produces high quiescent current levels will be considered as a defect.

In this paper, we further extend the approach proposed by S. Jandhyala, et all., [9-12]. The core of this approach lies in applying conventional cluster analysis techniques to I_{DDQ} testing. Each IC is represented as a point in an N dimensional space where N is the number of test vectors applied. In any given lot of ICs, a large number of ICs are generally good and a smaller number tend to have defects of various types. Using this characteristic, at the end of the process all the ICs are grouped into a set number of groups that has been determined a priori. All the ICs in a group tend to display similar current distributions over a range of test vectors applied, i.e. they tend to display the same quiescent current levels when compared for each vector. This approach does not rely on a fixed threshold for the quiescent current values. It also takes into account

the normal circuit operation states that display elevated quiescent current levels. In addition, this approach can provide a means of setting a threshold quiescent current level if so desired. In this paper we further extend this approach by making some recommendations on the number of clusters each lot ICs needs to be classified into, a mechanism to make a test decision on the ICs and approach to improve the quality of the test as per user requirements.

This paper is organized as follows: Section 2 introduces cluster analysis techniques and their uses. Section 3 provides an overview of the proposed approach and some background on the data used. Section 4 discusses the results obtained by implementing the suggested approach and their interpretation. Section 5 discusses the results of comparison between the proposed approach and the 'current signatures method' and concludes the paper.

2. Cluster Analysis

Cluster analysis in its simplest form can be defined as finding 'natural groups' within a large data set. Clustering is the process by which a collection of n objects, each of which is described by a set of p characteristics or variables, is divided into k number of groups ($k < n$). All the objects in a particular group will then display the same characteristics over the entire range of individual p variables. In this approach, n is the number of ICs in a lot, p is the number of I_{DDQ} test vectors applied and k is the number of groups or clusters formed at the end of the process. The purpose of clustering is to uncover any hidden structure or pattern that resides in the data and a further study is needed to achieve the end result, in this case a test decision.

2.1 Clustering Algorithms

The number of groups that are to be formed and the basis for this classification is a function of the specific clustering algorithm used and can be customized to fit a particular application. Clustering involves a correlation or other such measure of association for forming groups of objects. There are several such measures, for example, 'Angular Separation', 'City Block', 'Euclidian Distance', the most common being the 'Euclidian Distance'. The algorithm chosen for this application was the 'K-Means' algorithm. The advantages associated with the 'K-Means' algorithm are its robustness, the ability to specify the number of clusters, the algorithms treatment of the outliers, relative simplicity of the algorithm and its minimal use of the computing resources [11]

2.1.1 K-Means Clustering Method

In the K-Means method, individual data points are partitioned into clusters such that each data point belongs to the cluster whose center is closest in terms of 'Euclidian' distance. The cluster centroid is calculated on the basis of the cluster's current membership rather than it's membership at the end of the last reallocation cycle. The algorithm initially forms a predetermined set of seed points. The final number of clusters specified determines this number of seed points. Each seed point is classified as a cluster. All the data points are then assigned to a cluster with the nearest centroid. The cluster centroid is then updated and the data points reallocated. This process repeats until there are no further changes in the cluster membership.

2.2 Cluster Application

The cluster analysis can be performed using several methods. There are several publications containing details on the algorithms, their applications and their characteristics. Using this information, writing 'C' code to implement the chosen algorithm is a fairly simple process. There are also several commercial off the shelf statistics software packages that have already implemented these algorithms. The two most common are 'SAS' and 'SPSS'. The software package used for cluster analysis in this paper was SPSS.

3. I_{DDQ} Testing and Cluster Analysis

In the proposed approach, the I_{DDQ} measurements collected after applying the test vectors are formatted to translate the data into a format acceptable by the statistical tool. This data is then subjected to cluster analysis. The results of the cluster analysis are then used to classify the devices as either good or defective. The results can also be further analyzed to make changes either in the design or to the manufacturing process thus improving yield.

3.1 Background on the Data used

The proposed approach was applied to I_{DDQ} data collected on a high volume device manufactured in a deep sub micron process at Texas Instruments [9-12]. The device contains $\cong$650K gates and has extensive DFT features including full scan. All the vectors that were applied while obtaining the I_{DDQ} measurements were generated using a commercially available ATPG tool.

For the purpose of our work, 30 I_{DDQ} measurements were taken on 4 lots containing 627, 716, 725 and 798 devices. A fault coverage of 95% (stuck-at fault model) was obtained using these 30 vectors. Also due to the

constraints of space, the results obtained by applying the proposed approach on only one lot are provided.

3.2 Number of Clusters

The number of clusters the ICs to be divided into is specified at the start of the process. Once the clustering process has completed, the minimum, median and maximum I_{DDQ} current values are plotted for the cluster containing the most number of ICs. If the I_{DDQ} values satisfy the following criterion

$$(I_{max} - I_{med}) \leq 3 (I_{med} - I_{min}) \quad - \quad (1)$$

where I_{max} is the maximum I_{DDQ} current value among all the ICs in that lot, I_{med} is the median I_{DDQ} current value for all the ICs in that lot and I_{min} is the minimum I_{DDQ} current value among all the ICs in that lot, then no further clustering is required. If the above criterion is not satisfied with the initial number of clusters then the number of clusters is increased by a factor of two and clustering is repeated.

Alternatively, the test engineer can view the formatted results of the clustering process to make a decision if further clustering is required. In this approach, the ratio of the (I_{max} - I_{med}) to the (I_{med} - I_{min}) is plotted for all the clusters. This ratio can also be termed as the cluster tightness. Depending upon the test engineer's quality and yield requirements, a decision can then be made as to whether further clustering is required.

3.3 Test Decision

A test decision is made on a cluster-by-cluster basis as opposed to an IC-by-IC basis. That is if a cluster is considered good, then all the ICs in that cluster are classified as good and vice versa. In order for a cluster to be classified as good, two criteria have to be met

$$I_{mean} \leq (\mu + x\,\sigma) \quad - \quad (2)$$
$$I_{max} \leq 4(\mu + x\,\sigma) \quad - \quad (3)$$

where I_{mean} is the mean of all the I_{DDQ} current values for all the ICs in the cluster, μ is the mean of all the I_{DDQ} current values for all the ICs in the lot, σ is the standard deviation for all the I_{DDQ} current values for all the ICs in the lot and x is a quality factor. The quality factor affects the yield as well as the quality of the test process. A lower quality factor will decrease yield but fewer bad test decisions are made on defective ICs.

A test engineer can also view the formatted results of the cluster analysis and make a test decision on each cluster. In this approach the ratio of % rejection is plotted against

the I_{DDQ} value. The test engineer can then make a test decision visually. The advantage to this approach is that the engineer can make a decision based on his yield requirements without compromising the test quality.

4. Results

The results obtained after applying the above approach to a lot containing 725 ICs are provided below. Initially the number of clusters was set at 5. This number was not sufficiently high enough to satisfy (1). The number of clusters was then progressively increased from 5 to 10 and then 20. The cluster analysis performed with number of clusters set at 20 provided acceptable results. The test decision process also became substantially easier with 20 clusters. The interim results obtained with the cluster number set to less than 20 are also provided.

4.1 5 Clusters

This section discusses the results obtained after cluster analysis with all the 725 devices classified into 5 clusters. Figure 1 shows the distribution of the I_{DDQ} currents over 5 clusters. On the X-axis, the number of devices grouped into each cluster is shown. On the Y-axis, the I_{DDQ} distribution of all the devices in that cluster is shown. To protect proprietary data, we have normalized the I_{DDQ} values in this paper, hence the absence of units for I_{DDQ} values. This is a range as opposed to a single value due to the fact that all the measurements across 30 vectors are being depicted. The minimum, maximum and median I_{DDQ} values are also shown in the figure. This is a range as opposed to a single value due to the fact that all the measurements across 30 vectors are being depicted. The minimum, maximum and median I_{DDQ} values are also shown in the figure with the block corresponding to the maximum value, the diamond to the minimum and the dash to the median value.
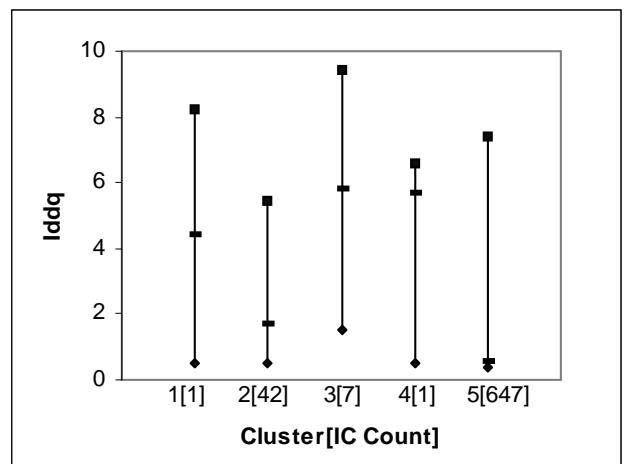
Figure 1: 5 Cluster Statistics

Assuming that the majority of the ICs in the lot were probably good and a small percentage being defective, it is difficult to make a test decision on any of the clusters by looking at figure 1. There is no cluster that has a current distribution markedly different from the other clusters.
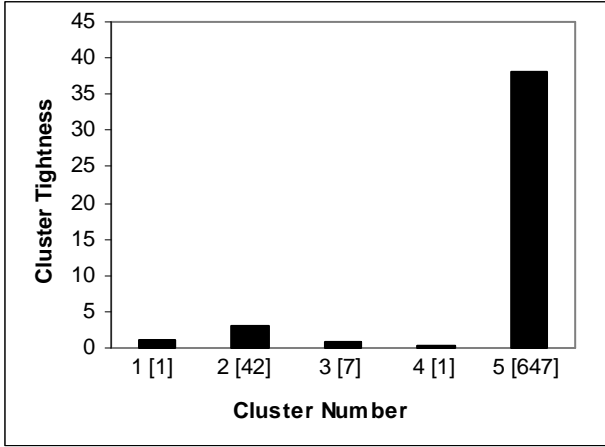

Figure 2: 5 Cluster Tightness

It is obvious from figure 2 that the largest cluster (5) is not very tight. Thus the decision to perform further cluster analysis with an increased number of clusters is the logical extension to this exercise.

Even though a majority of the ICs in the lot were classified into cluster 5, given the fact that the minimum and median I_{DDQ} current values for this cluster are very low and the difference between them is minute, the maximum I_{DDQ} current value is very high and difference between the median I_{DDQ} and the maximum I_{DDQ} currents is unacceptable. Hence cluster 5 cannot be classified as being good.

The logical explanation for this anomaly would be that there is an IC whose current distribution over the majority of the vectors closely mirrored the current distributions of the other ICs in the same cluster but there was defect that was being excited by a few vectors, possibly as few as 1 vector. Such an IC is termed as an outlier. Again this points to the need for further clustering.

4.2 10 Clusters

This section describes the results obtained after classifying ICs from the same lot into 10 clusters. All the descriptions for the tables and the figures are the same as those discussed for the results obtained after clustering

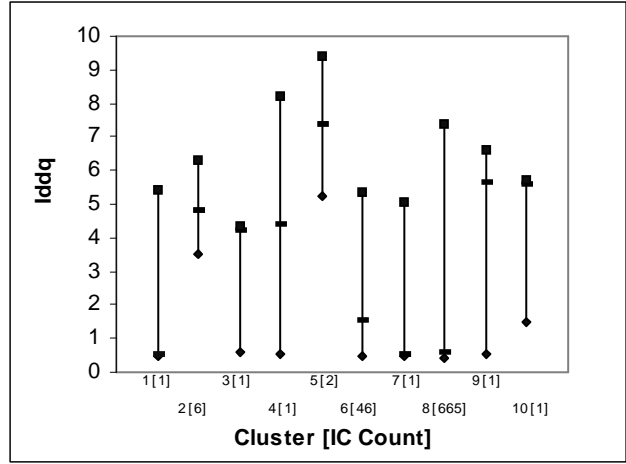into 5 clusters and for purposes of brevity have not been repeated in this section.

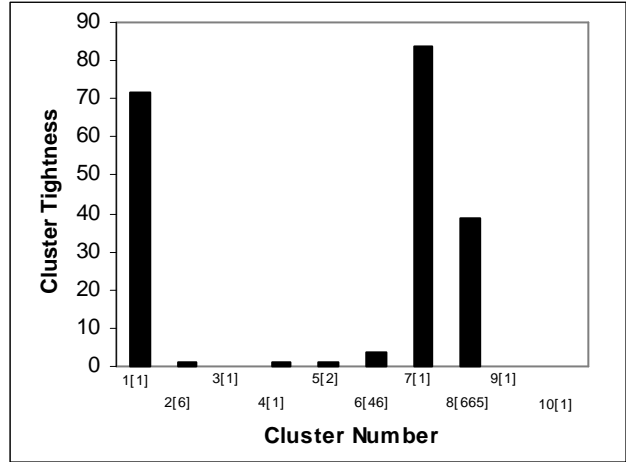**Figure 3: 10 Cluster Statistics**

Figure 4: 10 Cluster Tightness

As can be seen from figures 3 and 4, there was an improvement in the results obtained after cluster analysis. This can be easily explained by the fact that as the cluster number is increased progressively, the outliers that would have otherwise been classified into a larger cluster are now classified into a cluster on their own. While some clusters (1, 2, 3, 4, 5, 7, 9 and 10) can easily be identified as containing defective ICs, the largest 2 clusters, 6 & 8, while having a low minimum and median I_{DDQ} current values, are still not tight enough. In other words, the maximum I_{DDQ} current values are still beyond the acceptable range. A few outliers that need to be classified into a different cluster cause these elevated levels of I_{DDQ} currents. Thus further cluster analysis is required to flush out these outliers and obtain a set of clusters that can be easily classified as either good or defective.

4.3 20 Clusters

This section describes the results obtained after classifying ICs from the same lot used before into 20 clusters. All the descriptions for the figures are the same as discussed in section 4.1 and for purposes of brevity have not been repeated in this section.
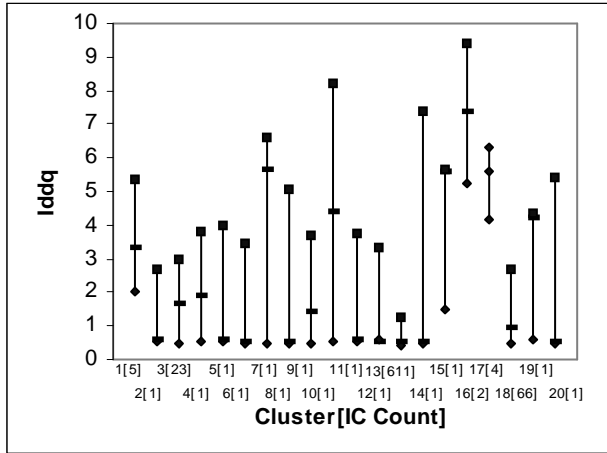

Figure 5: 20 Cluster Statistics

As we can see from figure 6, the 3 largest clusters (3, 13 & 18) are also among the tightest clusters. Further, these 3 clusters have relatively low maximum IDDQ current values. This negates the need for further clustering.
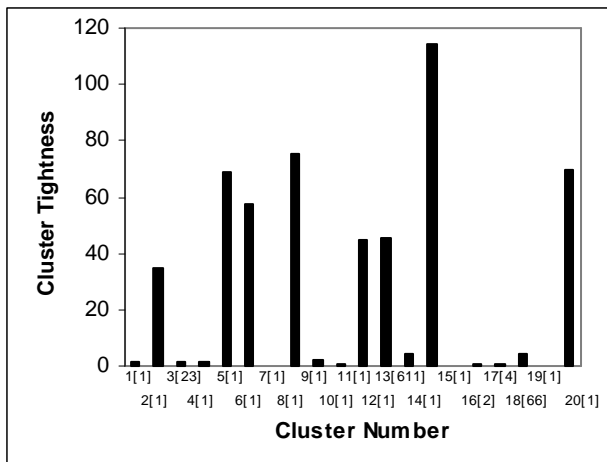

Figure 6: 20 Cluster Tightness

In order to make a test decision, the test engineer can use one of two methods. He can either use equations 2 and 3 or make a test decision after visual inspection of the data.

While making a test decision on the clusters using equations 2 and 3, the test engineer has to set to determine the value of the quality factor. To make the least amount of bad test decisions, this value has to be set to 1. In order to meet yield requirements, this value can be incremented but will potentially lead to bad test decisions. In this exercise, both the test decision approaches classified cluster 3, 13 and 18 as being good and the rest defective.
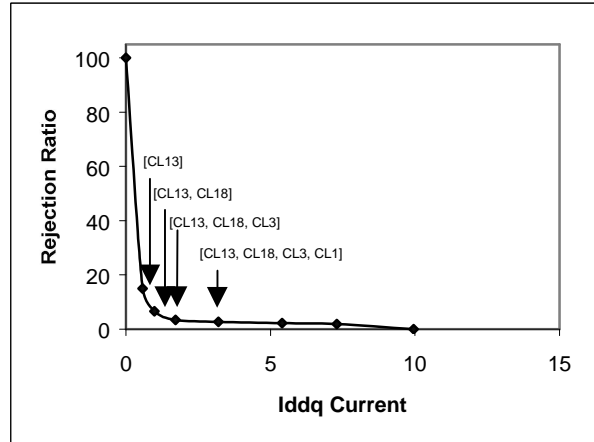

Figure 7: Rejection Ratio vs. I_{DDQ} Current

Figure 7 shows a plot of rejection ratio vs. I_{DDQ} mean current values. The percentage of devices rejected is plotted along the y-axis and the mean I_{DDQ} current of the good devices is plotted on the x-axis. If only cluster 13 is classified as being good and the rest as defective, then the rejection ratio is 15%, that is 15% of all the ICs in this lot were classified as defective. The mean I_{DDQ} current for all the ICs in this cluster is 0.58. If clusters 13 and 18 are classified as good, then rejection ratio drops to 6.6%. The mean I_{DDQ} current of the good devices goes up to 0.99. The test engineer can use such a plot to select a threshold I_{DDQ} current value for traditional I_{DDQ} testing. He/she can also monitor real time, the improvements in yield and mean I_{DDQ} currents as the number of clusters being classified as good increases or decreases. For example, the mean I_{DDQ} current goes up from 0.99 to 1.72 and the rejection ratio drops to 3.4% if cluster 3 was classified as good along with clusters 13 & 18. If cluster 1 was also classified as good, then the increase in mean I_{DDQ} current is significant while offering very little improvement in the rejection ratio. Thus for this exercise, cluster 1 was classified as defective.

The exercise was then repeated on 3 other lots of the same IC and the results were very similar to the results obtained for this lot.

5. Comparison and Conclusions

The fundamental drawback of the 'current signatures' approach proposed by A. Gattiker, et al [6] is its inability to distinguish between elevated I_{DDQ} currents produced by normal, non defective circuit operation and the elevated I_{DDQ} currents produced by a defect in an IC. This became further obvious when the proposed approach was compared to the 'current signatures' method. The number of ICs rejected by the current signatures approach was 52 as compared to 25 ICs rejected by the proposed approach. The rejection ratio for the 'current signatures' method was 7.31%. Upon closer inspection of the ICs being classified as defective by the current signatures method and as good by the proposed approach, it was found that all these ICs were indeed displaying higher I_{DDQ} current values for a single vector. After further inspection it was found that all the ICs in the lot were displaying elevated I_{DDQ} currents for the same vector. Thus there were at least 100% more bad test decisions made while using the 'current signatures' method. Even though the rejection ratio was not significant in terms of numbers, it was twice that of the proposed approach and over the 4 IC lots, approximately 110 ICs were rejected that were actually classified as good by the proposed approach.

A more robust, innovative approach to I_{DDQ} testing was presented. The traditional I_{DDQ} testing approach treats each test vector in isolation and the current signatures approach treats each IC in isolation. The goal of this approach is to identify defective ICs while keeping the current distribution of all the ICs in the lot over a range of vectors in mind. With advances in process technology and the design techniques, such innovative I_{DDQ} test techniques are becoming essential to separate good ICs from defective ICs.

We have demonstrated that by applying clustering on the I_{DDQ} measurement data and following a few simple guidelines it is a fairly straightforward process to making a test decision. Also the proposed approach leads to fewer bad test decisions, hence increasing the yield.

Acknowledgements

References

[1]. L.K. Mourning, et al, " Measurement of Quiescent Power Supply Current for CMOS ICs in Production Testing", Proc. Of IEEE Int. Test Conf. 1987, pp. 300-309

[2]. C. F. Hawkins, et al, " Quiescent Power Supply Current Measurement for CMOS IC Defect Detection", Proc. Of IEEE Trans. On Industrial Electronics, 1989, pp. 211-218.

[3]. R. Perry, "I_{DDQ} Testing in CMOS Digital ASIC's – Putting it All Together", Proc. of IEEE Int. Test Conf. 1992, pp. 151-157.

[4]. T. W. Williams, et all, "I_{DDQ} Test: Sensitivity Analysis of Scaling", Proc, of IEEE Int. Test Conf. 1996, pp. 786-792.

[5]. Gattiker and W. Maly, "Current Signatures", Proc. Of IEEE VLSI Test Symp. 1996, pp. 112-117.

[6]. Gattiker, et all, "Current Signatures for Production Testing", Proc. Of IEEE Int. Workshop on I_{DDQ} Testing, 1996, pp. 25-28

[7]. C. Thibeault, "A Histogram Based Procedure for Current Testing of Active Defects", Proc. of IEEE Int. Test. Conf. 1999, pp. 714-723

[8]. C. Miller, "I_{DDQ} Testing In Deep SubMicron Integrated Circuits", Proc. Of IEEE Int. Test Conf. 1999, pp. 724-729.

[9]. S. Jandhyala, "Clustering Based Techniques for I_{DDQ} Testing", Proc. IEEE Int. Test Conf. 1999, pp. 730-737.

[10]. S. Jandhyala, "Clustering Based Techniques for I_{DDQ} Testing", M.S. Thesis, Colorado State University, 1998.

[11]. L. Kaufman and P. J. Rousseeuw, " Finding Groups in Data", John Wiley 1990