Design of CMOS Circuits for Stuck-Open Fault Testability

Anura P. Jayasumana, Yashwant K. Malaiya, and Rochit Rajsuman

***Abstract*—CMOS circuits present severe problems in the detection of transistor stuck-open faults. In CMOS circuits, the transistor stuck-open (s-open) faults cause sequential behavior, and hence two- or multipattern sequences are used to detect s-open faults. Furthermore, two- or multipattern sequences may fail to detect a fault in several situations. The available methods for augmenting CMOS gates require a large amount of extra hardware and still are not able to detect a fault deterministically. A new design is presented which requires a single transistor to improve the circuit testability. The proposed design is highly testable and ensures the detection of s-open faults while a single test vector is used during testing. These tests are not invalidated due to the timing skews, glitches, or charge redistribution among the internal nodes.**

I. Introduction

THE detection of a FET stuck-open fault requires a sequence of two test vectors instead of a single test pattern [1]–[9]. The first pattern is applied to initialize the output of a gate and the second pattern to detect the fault. For a stuck-open (s-open) fault in the n-part (p-part), the first pattern sets the output to logic ONE (logic ZERO). The second pattern then attempts to provide a low-resistance path between the output and the ground (power supply) through the faulty transistor. Robust two-pattern tests have been suggested to avoid test invalidation in the presence of timing skews. The Hamming distance between the initialization pattern and the second test pattern is kept at unity in these robust test sequences [4]–[6] and thus the possible intermediate state is avoided.

The generation of robust test sequences is a complex process. The requirement of large CPU time makes the test generation very costly. It is also possible that a combinational block may not have any two-pattern robust sequence [4], [5]. To overcome this problem, testable design schemes have been proposed [4]–[9]. These schemes employ extra transistors in fully CMOS (FCMOS) gates, to augment CMOS circuits for the detection of stuck-open faults. Fig. 1 shows the basic concepts of these schemes. The test-generation complexity for circuits shown in Fig. 1 is less compared to that of the FCMOS circuits. In all the circuits of Fig. 1, a two- or multipattern robust sequence can be obtained by appropriately controlling the signals C_p and C_n. However, because the circuits shown in Fig. 1 require two- or multipattern test sequences, glitches caused by the delays in the prior logic may invalidate the tests [10], [11]. The reason given in [11] and [12] is the presence of a high-impedance state during the last vector. A glitch during the last vector may violate the high-impedance state and hence invalidate the test. This result was given in the form of the following theorem [11].

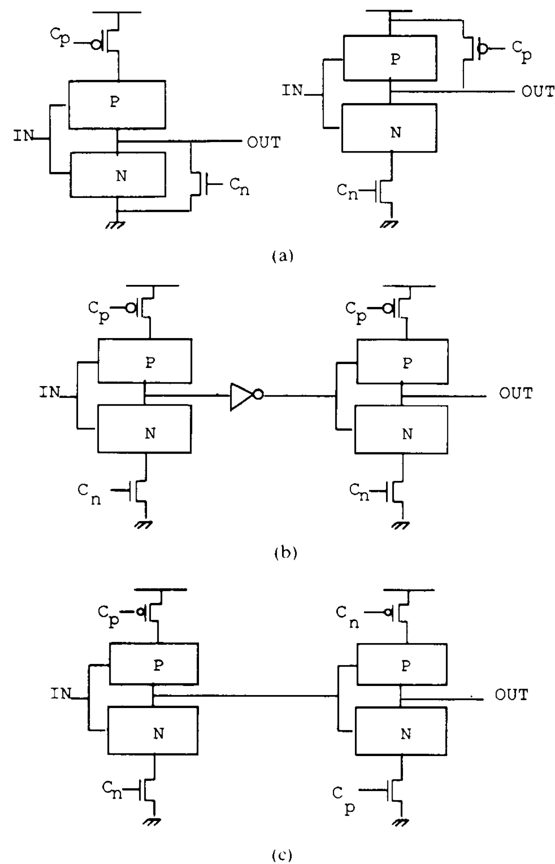

Fig. 1. (a) Testable CMOS gate proposed by Reddy *et al.* [4], [5]. (b) Testable CMOS design by Liu and McCluskey [7], [8]. (c) Testable CMOS design by Gupta *et al.* [9].

Theorem 1: In an FCMOS gate, except in a NOT gate, in at least one part (either the n-part or the p-part), all the FET s-open faults may remain undetected in the presence of circuit glitches, if two- or multipattern test sequences (even robust test sequences) are used. □

The standard techniques in digital circuits to eliminate the glitches is to enclose the two minterms with another product term that overlaps both the groupings. One extra gate in the circuit can generate the product term covering two adjacent minterms. This eliminates the possibility of a glitch at the output. However, the requirement of large extra hardware limits the use of such redundancy.

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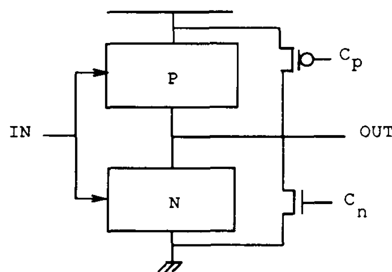


Fig. 2. Testable CMOS design proposed by Rajsuman *et al.* [10].

References [11] and [12] present a solution to this problem. The circuit shown in Fig. 2 overcomes this problem by avoiding the high-impedance state. A single test vector is used to detect s-open faults in the circuit shown in Fig. 2. During testing the circuit appears either as a pseudo-nMOS or a pseudo-pMOS gate, and hence the tests are not invalidated.

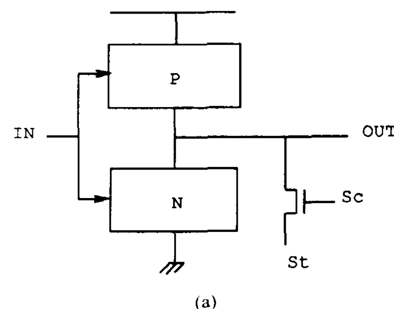
In [11] and [12], two extra transistors are used, controlled by two external signals (see Fig. 2). These extra transistors were scaled such that the resistance of these transistors, T_p and T_n, is considerably higher than the ON resistance of the n-part or p-part, respectively. During normal operation, these transistors are kept off by setting $C_p = 1$ and $C_n = 0$. During the testing of the n-part $C_p = C_n = 0$, and during the testing of the p-part $C_p = C_n = 1$. Effectively, during testing this augmented gate appears as a pseudo-nMOS (while testing n-part) or a pseudo-pMOS gate (while testing p-part). Hence, the test procedures that require a single vector are able to detect the faults.

The major disadvantage of the circuit shown in Fig. 2 is the requirement of two extra transistors controlled by the external signals. Although the extra hardware is comparable or less than the schemes shown in Fig. 1, it still is impractical to build such circuits. All the schemes shown in Figs. 1 and 2 require at least two extra transistors per gate. From all practical aspects, this is unaffordable. Furthermore, the requirement of two extra transistors also causes a reduction in the switching speed, because of the increased output capacitance.

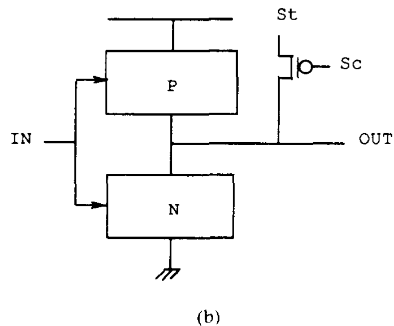
In the next section, we present a CMOS design that needs only one transistor to make the gate testable. The design allows the detection of a transistor s-open fault, while using a single test vector. It also simplifies the test-generation phase and reduces the testing cost. As a single test vector is used and the high-impedance state is avoided, the tests are not invalidated because of timing skews, glitches, or charge sharing.

II. New Design of Testable CMOS Gates

In the last section, we briefly reviewed the schemes available in the literature. While it is reported that the schemes shown in Fig. 1 are not suitable, the scheme shown in Fig. 2 is capable of detecting the faults deterministically. The main reason is the utilization of a single test vector, which avoids the high-impedance state during testing. The point to note here is that during the testing of the n-part, a 0 vertex is used (input vector under which the fault-free output is ZERO), which keeps the p-part OFF. During the testing of the p-part, a 1 vertex is used (input vector under which the fault-free output is ONE), which keeps the n-part OFF. During testing of the n-part, the extra transistor controlled by C_p brings logic ONE at the output in the presence of a fault. During the testing of p-part, the transistor controlled by C_n brings logic ZERO at the output in the presence of a fault.



(a)



(b)

Fig. 3. Proposed testable CMOS design using (a) nMOS transistor, and (b) pMOS transistor.

The same functionality of these two extra transistors can be achieved by a single pass transistor. The switching of this pass transistor is controlled by an external signal S_c and the value passed is provided externally by the signal S_t. Thus, we still use two external control signals. However, in this design we require only one extra transistor. The scheme is shown in Fig. 3. A single nMOS or pMOS transistor is used at the output node. Fig. 4 shows the conversion of the gate during test mode. If an nMOS transistor is used, then during the normal operation S_c is set to ZERO. It should be noted that in Fig. 3(a) an nMOS transistor is used. The same functionality can be obtained by a pMOS transistor as in Fig. 3(b). If a pMOS transistor is used, then during the normal operation $S_c = 1$ and during the test mode $S_c = 0$. The advantage of using an nMOS transistor is that the size of an nMOS transistor is small in comparison to a pMOS transistor while offering the same resistance.

This extra transistor provides a static load at the output. The dimension of this extra transistor should be chosen such that the ON resistance of this transistor is considerably higher than the ON resistances of the n-part as well as the p-part. With the nMOS transistor, for example, when $S_c = 1$ the gate is essentially transformed to an nMOS or a pseudo-pMOS gate. Therefore, the standard rules in designing pseudo-nMOS (pseudo-pMOS) type structures can be used to determine the size of the extra transistor. In general, a minimum-size transistor, which offers a resistance of about 5–6 times

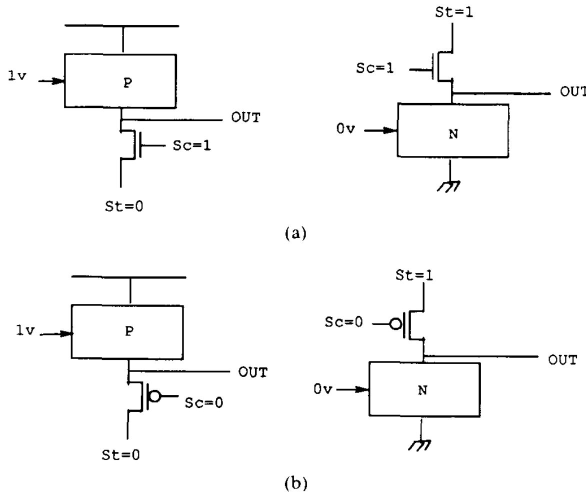


Fig. 4. Augmented CMOS gate using (a) nMOS transistor and (b) pMOS transistor during test mode.

higher than the ON resistance of the p-part, is sufficient to provide the correct voltage levels.

With the proposed augmentation, any s-open fault can be detected by a single test vector. The results are given as follows.

Theorem 2: By augmenting an FCMOS gate as shown in Fig. 3, any single s-open fault in the functional part can be detected by a single test vector. These tests are not invalidated by timing skews/delays, glitches, or charge redistribution.

Proof: Consider an s-open fault in the n-part. The test vector for this fault is $S_c = S_t = 1$, and a zero vertex (0v) covering the interested nMOS transistor. The 0v will turn the p-part OFF. Therefore, the augmented gate will appear as a pull-down n-part and a pull-up T_n. If a fault is present, it will cause a high-resistance path between the output and the ground. Hence, the output will appear as logic ONE. If the fault is not present, 0v will provide a low-resistance path from the output to the ground. As the ON resistance of T_n is considerably higher than the ON resistance of the n-part, the output will appear as logic ZERO. Therefore, a single test vector will detect the fault.

Similarly, it can be shown that $S_c = 1$, $S_t = 0$, and a 1v, covering the interested pMOS transistor, can detect the pMOS s-open fault. It should be noticed that a single test vector is required to detect the fault. The test vector brings the output node to a definite logic level and does not create a high-impedance state. If a glitch appears during testing, although the output value may change momentarily, the steady-state value will not be affected. The output voltage will recover after the glitch due to the path through the extra transistor T_n. Hence, the test cannot be invalidated by timing skews/delays, glitches, or charge redistribution. In the traditional FCMOS designs (as well as in schemes shown in Fig. 1), such a glitch could charge or discharge the output node spuriously. In FCMOS, the output does not recover after the glitch because the second pattern creates a high-impedance state. QED. □

Theorem 3: In the augmented CMOS gate shown in Fig. 3, a test set which detects all single s-open faults in the functional transistors will also detect all multiple s-open faults in the functional part.

Proof: Suppose there is a multiple fault P, which is a set of n single simultaneous faults, i.e.,

$$P = \{p_1, p_2, \cdots, p_n\}.$$

A test sequence which detects all single faults will fail to detect the multiple fault P only if the following condition holds:

$$E_{ff}(p_k) = E'_{ff}(P - p_k)$$

where E_{ff} represent the effect of the fault.

The whole test set for the augmented gate can be divided into two subsets. One subset detects s-open faults in the n-part and the other subset detects s-open faults in the p-part. A test vector switches off all the conduction paths and attempts to activate one conduction path from the output to the ground (for the testing of n-part), or the output to the power supply (for the testing of p-part). Hence all stuck-open faults in that conduction path are detectable by this vector. If a multiple open fault involves two or more conduction paths, two or more vectors are able to detect the fault. As we are considering only stuck-open faults, one fault cannot mask the effect of other faults. QED. □

Theorem 4: The functional transistors in an augmented gate, as shown in Fig. 3, can be tested for all single and multiple s-open faults by a sequence of maximal length $2n$, where n is the number of transistors in the unaugmented n-part or p-part.

Proof: For testing the augmented gate for s-open fault, a 0v (for the n-part) or a 1v (for the p-part) is applied. These 0v or 1v are chosen such that they cover the FET of interest. Generally a number of FET's are covered by a single vector. For the worst case, when only one FET is covered by one vector, we need at most n test vectors to test one part. Thus, to test the complete gate for all single s-open faults, at most $2n$ vectors are required. From Theorem 4, the same test set will also detect all multiple s-open faults in the functional transistors. QED. □

Theorem 4 gives an upper bound for the length of the test sequence. In general, the length of the test sequence is much smaller. This is mainly due to the fact that a test vector examines the continuity of a path from the output to the ground/power supply. A number of transistors get tested by a single test vector. For example, the test set for a primitive gate (NAND, NOR, NOT) has only $(n+1)$ vectors.

It should be noted that the additional transistor cannot be tested in this design. However, an open fault in the extra transistor is benign and does not affect the normal circuit operation. Also, the single-fault assumption implies that the extra transistor is fault free if a fault exists in the functional part and vice versa.

III. Advantages of Proposed Design

There are several advantages of the proposed CMOS design. Table I compares the proposed design with the existing techniques. The most important aspect is that the proposed design requires a very small amount of extra hardware for testing. This factor makes this design practical for actual implementation. Furthermore, because this scheme requires only a single transistor at the output, the increase in the output capacitance is negligible. While all the existing

TABLE I
COMPARISON OF PROPOSED SCHEME WITH THE EXISTING SCHEMES

Schemes	test vectors	Extra hardware	Problems by glitches
Ref. [4], [5]	2	2 FET's + 2 controls	yes
Ref. [7], [8]	2	2 FET's + 2 controls + 1 inverter	yes
Ref. [9]	2	2 FET's + 2 controls	yes
Ref. [11]	1	2 FET's + 2 controls	no
Proposed	1	1 FET + 2 controls	no

schemes have a significant penalty in switching speed due to the use of two transistors, the proposed scheme offers almost no penalty in switching speed.

Another major advantage of this design is the high testability. All single and multiple s-open faults in the CMOS gate can be detected by a single test vector. This reduces the testing time drastically. It reduces the test application time by almost 50% as it uses a single test vector instead of a sequence of two vectors. Use of a single test vector also eliminates the complexity in test generation. Complexity in generating two- or multipattern sequences is a major cost factor in testing CMOS circuits. This complexity and the cost associated with generating robust test sequences is even higher.

As only a single pattern is required to test a given fault, the tests for the augmented gates can be generated by simple procedures. All the classical algorithms such as the D-algorithm, PODEM, and automatic test-pattern generating programs (ATPG's) for nMOS can generate the test for such augmented gates. The scheme detects the stuck-open faults deterministically and ensures the detection irrespective of the problems identified in [4]–[10]. Also, the proposed scheme offers significant advantage for random or pseudorandom testing procedures. Random testing is very inefficient for the detection of stuck-open faults in the FCMOS designs. This is because the probability of fault detection depends on two successive vectors.

Some of the existing testable design schemes such as those proposed in [4] and [5] are not suitable for multilevel circuits. This is mainly due to the problems associated with the propagation of the fault effect to the circuit output. The proposed scheme is free from this drawback. As the scheme uses a single test vector and none of the gates show a high-impedance state, the effect of a fault is propagated without any problem. In fact, testing of CMOS gates by this procedure can be compared with the testing of nMOS gates.

A disadvantage in the proposed design is the slightly higher power dissipation during testing. However, as this occurs only during testing, it is not a significant disadvantage.

IV. CONCLUSIONS

A new CMOS design is presented that offers highly testable CMOS circuits. The design requires a minimal amount of extra hardware for testing. The test phase for the proposed design is simple and uses a single test vector to detect a fault. The design offers the detection of transistor stuck-open faults deterministically. In the proposed design, the tests are not invalidated due to timing skews/delays, glitches, or charge redistribution among the internal nodes.

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