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Input Pattern Classification for Transistor Level Testing of BiCMOS Circuits*

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Abstract

In BiCMOS, transistor stuck-OPEN faults exhibit delay faults in addition to sequential behavior. Stuck-ON faults cause enhanced I_{DDQ}. The faulty behavior of Bipolar (TTL) and CMOS logic families is compared with BiCMOS. The faults in BiCMOS devices cause one or more parts (p-part or n-parts) of the circuit to exhibit a different state (conducting or non-conducting) from the fault-free circuit. An input pattern classification scheme is presented for different faults. These classes of patterns are then used to obtain test sets.

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1 Introduction

With the inherent advantages of CMOS and bipolar, BiCMOS is emerging as a major technology for many high performance digital and mixed signal applications. BiCMOS offers the following advantages [1]; improved speed over CMOS, lower power dissipation compared to bipolar, flexibility in I/O (TTL, ECL, CMOS compatibility), high performance analog capability and latch up immunity.

Transistor level shorts and opens model many of the physical failures and defects in ICs. The major fault models at transistor level are stuck-at faults, and shorts and opens of transistors and interconnects. It has been shown [2]-[7] that the stuck-at model does not cover many of the manufacturing defects in BiCMOS devices and that most open faults manifest themselves as delay faults. Analysis on the effects of bridging faults in BiCMOS is given in [3, 8, 9]. Reference [7] presents testability analysis and fault modeling of BiCMOS circuits in which the behavior of BiCMOS under faults is compared with CMOS. The most common type of BiCMOS circuits employ bipolar transistors to perform the function of driving output loads and CMOS to perform logic functions.

In this paper, since BiCMOS technology combines the advantages of both CMOS and bipolar, we compare the faulty behavior of BiCMOS with CMOS and bipolar. The faults in BiCMOS device causes the p-part or n-parts to exhibit a different state, conducting or non-conducting, from the fault-free circuit. A classification scheme for input patterns is presented for different faults. The classes of input patterns obtained are then used to obtain test sets for detection of the various faults in BiCMOS circuits. The tests so derived for one logic gate can then be used to generate the appropriate primary input patterns.

This paper is organized as follows. Comparison of the faulty behaviors of the three logic families (TTL, CMOS and BiCMOS) are done in section 2. Section 3 deals with manifestations of faults and input pattern classification in BiCMOS devices. Section 4 deals with generation of test sets for detection of the various faults in BiCMOS circuits. Derivation of input pattern classes is given in section 5. Finally, conclusions drawn from the study are given in section 6.

2 Comparison of BiCMOS with CMOS and TTL

BiCMOS circuits employ one or two Bipolar Junction Transistors (BJTs) to perform the function of driving output loads and CMOS to perform logic functions. Block diagram of a general Single

Figure 1: A general S-BJT BiCMOS device

BJT (S-BJT) BiCMOS device is shown in Figure 1. An S-BJT BiCMOS gate consists of CMOS p- and n-parts to perform logic function, a BJT and a pull-down n-part for driving the output load.

Summary of faulty behavior of single BJT BiCMOS, CMOS and TTL NAND devices is given in Table 1. Analysis of BiCMOS as well as CMOS and TTL NAND & NOR are given in [6]. A test generation methodology and a testable design for BiCMOS circuits are presented in [10] and [11] respectively. Response of the respective devices is evaluated for hard failures of the components (MOS & bipolar transistors and resistors). All possible failures such as, stuck-ON and stuck-OPEN of transistors, opens and shorts between terminals are considered.

The manifestations of faults in BiCMOS devices that are summarized in Table 1 are, logic testable, delay testable and current testable. Logic testable faults are faults that can be detected at logic level. Delay testable faults are those faults that exhibit delay in its output response. Generally, two or or multi-pattern sequences are used to detect delay faults. Some faults in BiCMOS devices exhibit enhances I_{DDQ} and these are classified as current testable faults. While some current testable faults can be detected by logic monitoring, some can be detected only by I_{DDQ} monitoring.

From Table 1, the conclusions that can be drawn are given below. While faults in TTL devices manifest either as logic testable or indeterminate output, in CMOS devices they exhibit either as

Table 1. Summary of faulty behavior in BiCMOS, CMOS and Bipolar(TTL) NAND Gates.

Summary of BiCMOS, CMOS & TTL NAND gates			
Type of faulty Behavior	BiCMOS NAND (S-BJT)	CMOS NAND	TTL NAND
Fault-free	—	—	**12(29%)**
Indeterminate	—	—	**4(10%)**
Logic Testable:	**18(33%)**	**16(50%)**	**25(61%)**
Stuck-at-0 or 1	10(18%)	8(25%)	25(61%)
Sequential Behavior	8(15%)	8(25%)	—
Delay Testable:	**10(19%)**	—	—
Current Testable:	**26(48%)**	**16(50%)**	
Logic Testable	17(31%)	14(44%)	—
Not Logic Testable	9(17%)	2(6%)	—

logic testable or current testable faults. 25% of the faults in CMOS devices manifest as stuck-at and 25% as sequential behavior. Out of the 50% of the faults in CMOS NAND which manifest as current testable faults, 44% in CMOS NAND are logic testable. However, 6% of the current testable faults in CMOS NAND devices are not logic testable, which means that only I_{DDQ} testing would detect the faults in a definite way. About 48% of the faults in single BJT NAND devices manifest as current testable faults, out of which almost 17% of the faults are not logic testable and hence, for these faults, only I_{DDQ} monitoring would ensure detection. 19% of the faults in S-BJT NAND are delay fault testable.

From the above summary on the behavior of S-BJT BiCMOS devices vis-a-vis CMOS and TTL devices, it can be seen that a major portion of the faults in S-BJT devices manifest either as current testable faults or as delay testable fault. This makes I_{DDQ} testing as well as delay testing methodologies important for BiCMOS devices. Current monitoring techniques [12, 13, 3] can be used to detect such faults. A scheme for current monitoring (I_{DDQ}) for BiCMOS devices is presented in [5]. In addition to current testable faults, BiCMOS devices exhibit delay testable faults too. Hence, the strategy for testing of BiCMOS devices are much more complicated than CMOS and TTL devices. Manifestations of faults and test generation in BiCMOS devices are addressed in the next sections.

Table 2. Summary of manifestations of faults in BiCMOS gates.

Summary	
Fault type	Manifestation
Any transistor Stuck-ON	Enhanced I_{DDQ}
p-part Stuck-OPEN	Sequential Behavior
n-part(1) Stuck-OPEN	Delay Fault
n-part(2) Stuck-OPEN	Sequential Behavior
Q_1 e/b OPEN	Stuck-at Behavior
Q_1 c OPEN	Delay Fault

3 Manifestations of faults

The results obtained under various stuck-on and stuck-open faults for a general S-BJT BiCMOS gate shown in Figure 1 is summarized in Table 2. A stuck-ON fault of any of the transistors in the S-BJT BiCMOS gate manifests as enhanced I_{DDQ} being drawn by the device for one or more input vectors. Hence, I_{DDQ} monitoring would detect the failure mode. A stuck-OPEN fault in the p-part or n-part(2) exhibits sequential behavior. Delay faults are observed for stuck-OPEN faults in n-part(1) or for Q_1 collector open fault. Bipolar transistor emitter or base open faults manifests as stuck-at-0.

In this section, we classify the input patterns according to the effect on the output in the presence of a fault. A section of the BiCMOS gate [p-part, n-part(1) or n-part(2)] is either conducting or not conducting for a given vector. Let P_t denote the set of vectors which turn ON the p-part. Similarly, let N_{1t} and N_{2t} denote the set of vectors which turn ON the n-part(1) and n-part(2) respectively. N_{1t} and N_{2t} are equivalent, and equal to the complement of P_t as shown in Figure 2(a). P_t^f, N_{1t}^f and N_{2t}^f are the set of vectors which turn ON the p-part, n-part(1) and n-part(2) respectively in the presence of fault f in that part. An input vector, when applied to a fault-free BiCMOS gate causes a conduction path in the p-part(V_{DD} to output and base of bipolar) or in n-part(1)(base of bipolar to Ground) and n-part(2)(output to Ground). Here, we are considering irredundant gates such that, for each transistor there is at least one input vector for which all the conduction paths are through that transistor. This condition may not be true, for example, for high drive cells where many transistors with the same gate input are connected in parallel.

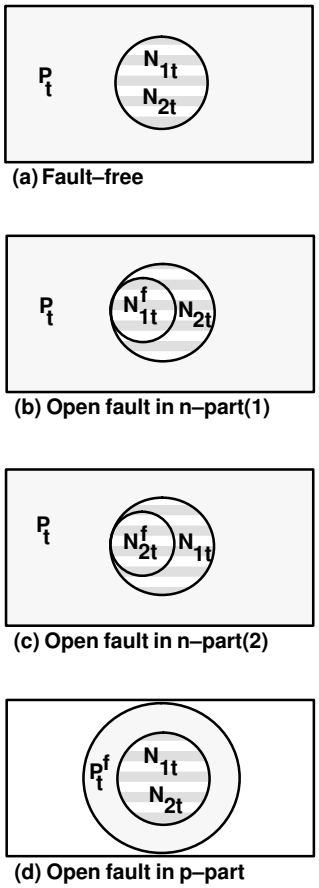

Figure 2: Venn diagrams for BiCMOS stuck-OPEN faults.

Below we give a series of lemmas that summarize the impact on the sets P_t, N_{1t}, N_{2t} due to the different faults.

Lemma 1: The set of vectors (N_{1t}^f) that cause the n-part(1) to turn ON in a BiCMOS gate with a stuck-OPEN fault f in n-part(1) is a proper subset of the set of vectors (N_{1t}) that turn ON the n-part(1) in the absence of the fault, i.e., $N_{1t}^f \subset N_{1t}$.

Proof: Consider an input pattern $\underline{t} \in N_{1t}^f$. As N_{1t}^f is the set of vectors which makes the n-part(1) conduct, there is at least one conduction path through the n-part(1) part for this vector. However, as f is a stuck-OPEN fault (for example, in transistor T), this conduction path cannot be through the transistor T. As we use the single fault assumption, only transistor T has a fault, and therefore the conducting path is not due to the fault. Thus the vector $\underline{t}$ will cause this path to conduct in the fault-free circuit as well, i.e., $\underline{t} \in N_{1t}$. Thus if $\underline{t} \in N_{1t}^f$ then $\underline{t} \in N_{1t}$.

Now consider a vector $\underline{t}' \in N_{1t}$ such that the only conducting path through n-part(1) is through the transistor T. However, in the presence of f, the stuck-OPEN fault of transistor T, this path cannot conduct. Therefore $\underline{t} \notin N_{1t}^f$. Thus, there is at least one vector in N_{1t} that is not in N_{1t}^f. Thus, N_{1t}^f is a proper subset of N_{1t}.

QED

The relationships between different sets is illustrated in Figure 2(b).

Lemma 2: The set of vectors (N_{2t}^f) that cause the n-part(2) to turn ON in a BiCMOS gate with a stuck-OPEN fault f in n-part(2) is a proper subset of the set of vectors (N_{2t}) that turn ON the n-part(2) in the absence of the fault, i.e., $N_{2t}^f \subset N_{2t}$.

The proof given for Lemma 1 can be easily extended for n-part(2). The resulting set causing shrinking of the N_{2t}^f region in the Venn diagram is shown in Figure 2(c).

Lemma 3: The set of vectors (P_t^f) that cause the p-part to turn ON in a BiCMOS gate with a stuck-OPEN fault f in p-part is a proper subset of the set of vectors (P_t) that turn ON the p-part in the absence of the fault, i.e., $P_t^f \subset P_t$.

The proof given for Lemma 1 can be easily extended for the p-part. The resulting set P_t^f region is shown in Figure 2(d).

It may be noted that a vector which turns ON the conduction path in the p-part causes the bipolar transistor (Q_1) to turn ON, provided the bipolar transistor Q_1 is fault-free. Hence, no separate test vector is needed to turn the bipolar transistor ON. Faults in the bipolar transistor

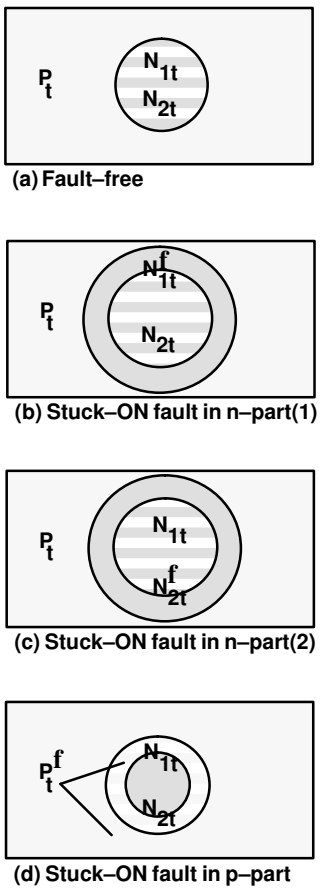

Figure 3: Venn diagrams for BiCMOS stuck-ON faults.

are addressed later.

Theorem: The set of vectors that cause the transistors in any part [n-part(1), n-part(2) or p-part] to turn ON in a BiCMOS gate with a stuck-OPEN fault in that part is a proper subset of the set of vectors that turn ON the corresponding part in the absence of the fault.

The proof of this theorem follows from the above lemmas.

Single stuck-ON faults are considered next.

Lemma 4: The set of vectors (N_{1t}) that cause the n-part(1) to turn ON in a BiCMOS gate is a proper subset of the set of vectors (N_{1t}^f) that turn ON the n-part(1) in the presence of the stuck-ON fault in n-part(1), i.e., $N_{1t} \subset N_{1t}^f$.

Following an argument similar to proof of Lemma 1, we can show that any vector in N_{1t} is also in N_{1t}^f. Now, consider a vector $\underline{t} \in N_{1t}^f$ which causes n-part(1) to provide a single conducting path through the transistor T containing the stuck-ON fault. As T is stuck-ON, there should be a vector $\underline{t}$ such that the gate voltage applied to transistor T is logic 0. This vector when applied to fault-free circuit will not cause n-part(1) to be conducting as it will turn T off. Thus $t \notin N_{1t}$. This completes the proof that $N_{1t} \subset N_{1t}^f$. The resulting N_{1t} region in the Venn diagram is shown in Figure 3(b).

Lemma 5: The set of vectors (N_{2t}) that cause the n-part(2) to turn ON in a BiCMOS gate is a proper subset of the set of vectors (N_{2t}^f) that turn ON the n-part(2) in the presence of the stuck-ON fault, i.e., $N_{2t} \subset N_{2t}^f$.

Lemma 6: The set of vectors (P_t) that cause the p-part to turn ON in a BiCMOS gate is a proper subset of the set of vectors that turn the p-part ON in the presence of the stuck-ON fault (P_t^f), i.e., $P_t \subset P_t^f$.

The proof given for Lemma 4 can be easily extended for n-part(2) and p-part. The resulting N_{2t} region and P_t region in the Venn diagrams are shown in Figures 3(c) and (d) respectively.

Theorem: The set of vectors that cause the transistors in any part(n-part(1), n-part(2) or p-part) to turn ON in a BiCMOS gate under fault-free condition is a proper subset of the set of vectors that turn ON the corresponding part in the presence of a stuck-ON fault.

The proof of this theorem follows from the above lemmas.

4 Test Sets for Fault Detection

With the above results, the test generation for BiCMOS devices can be done using the procedures given in the next subsections. Since the manifestations of the faults in the different blocks of p-part, n-part(1) and n-part(2) are known, appropriate test sets need to be generated to observe the manifestation of the respective faults at the output.

4.1 Test sets for stuck-ON faults

In the presence of a stuck-ON fault, the size of the sub-set of vectors turning the corresponding conduction paths ON increases, resulting in the expansion of the corresponding regions in the Venn diagram. Based on this result, tests facilitating I_{DDQ} testing for the various stuck-ON faults of a BiCMOS gate can be generated as given below.

The set of test vectors for a stuck-ON fault in the p-part is $\{P_t^f \cap (N_{1t})\}$.

The set of test vectors for a stuck-ON fault in the n-part(1) is $\{N_{1t}^f \cap P_t\}$.

The set of test vectors for a stuck-ON fault in the n-part(2) is $\{N_{2t}^f \cap P_t\}$.

The set of test vectors for a stuck-ON fault in the bipolar transistor is $\{N_{1t} = (N_{2t})\}$.

4.2 Test sets for stuck-OPEN faults

In the presence of a stuck-OPEN fault in any of the transistors, the number of the vectors turning the corresponding conduction paths ON decreases relative to that of fault-free circuit resulting in the shrinking of the corresponding regions in the Venn diagram. Testing of stuck-OPEN faults require two-pattern test $<t_1,t_2>$ to be applied. For detection of an s-OPEN fault in the p-part(n-part), the first pattern sets the output to logic ZERO(logic ONE). The second pattern then attempts to provide a low resistance path between the output/base of bipolar and the power supply(Ground) through the faulty transistor. Let the set of possible vectors for t_1 and t_2 be $\{T_1\}$ and $\{T_2\}$ respectively. Based on the above results, test sets $<t_1,t_2>$ for the various faults can be identified using the following results.

For a stuck-OPEN fault in p-part, the possible sets of tests T_1 and T_2 are given by:

$T_1 = \{N_{1t}\} = \{N_{2t}\}$

$T_2 = \{P_t^f\}^c \cap \{P_t\}$

For stuck-OPEN fault in n-part(1), the possible sets of tests T_1 and T_2 are given by:

$T_1 = \{P_t\}$

$T_2 = \{N_{1t}^f\}^c \cap \{N_{1t}\}$

For stuck-OPEN fault in n-part(2), the possible sets of tests T_1 and T_2 are given by:

$T_1 = \{P_t\}$

$T_2 = \{N_{2t}^f\}^c \cap \{N_{2t}\}$

Since bipolar transistor emitter and base open faults manifest as stuck-at-0, a test which tests for stuck-at-0 would detect the fault. The possible test can be from $T = \{P_t\}$. Bipolar transistor collector open fault manifests as low to high delay fault and hence, two pattern test need to be applied. The possible sets of tests T_1 and T_2 are given by:

$T_1 = \{N_{1t}\}$

$T_2 = \{P_t\}$

5 Derivation of Input Pattern Classes

Logic behavior of single and double BJT BiCMOS devices under transistor level shorts and opens were presented in [3]-[6]. For a given fault f, if P_t^f, N_{1t}^f or N_{2t}^f can be found, then the test vector can be selected according to the procedure given in the previous section.

With the above observations, test sets for S-BJT BiCMOS devices can be obtained using the procedure given in the previous section. Since the manifestations of faults in the different parts (p-part, n-part(1) and n-part(2)) are known, appropriate test vectors need to be generated to observe the manifestation of the respective faults at the output.

In this section, we show how the sets P_t, P_t^f, N_{1t}, N_{1t}^f, ... etc. can be derived for different faults under the assumption that a primary input of a gate is connected only to one transistor gate in each part. However this can be extended to the more general case by assigning literals to denote gate inputs of each transistor.

Below we consider the faults in n-part(1). Let $f(x)$ be the function implemented by this part, where $\underline{x} = \{x_1, x_2, ... x_n\}$ and x_i is the gate input to the ith transistor. For example, for the n-part shown in Figure 4, $\underline{x} = \{A, B, C, D, E\}$ and $f(\underline{x}) = (A+B)C(D+E)$.

Let $g(\underline{x},x_i) = f(x_1, ... x_{i-1}, 1, x_{i+1}, ... x_n)$

and $h(\underline{x},x_i) = f(x_1, ... x_{i-1}, 0, x_{i+1}, ... x_n)$

For the example, $g(\underline{x},D) = (A+B)C$ and $h(\underline{x},D) = (A+B)CE$

Lemma 7: For a stuck-ON fault in transistor x_i, the set N_{1t}^f is given by

$N_{1t}^f = \{\underline{x} \mid g(\underline{x}\ , x_i) = 1\}$

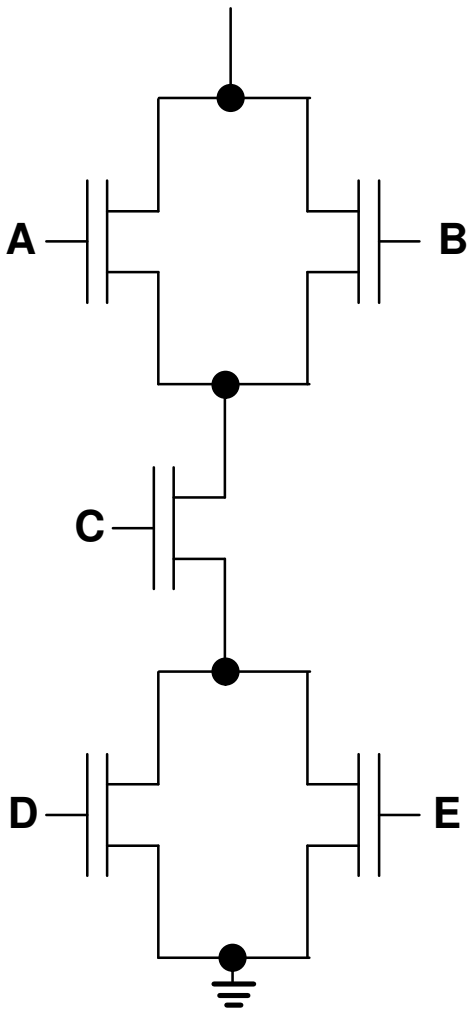

Figure 4: n-part of a BiCMOS gate for Example in section 5.

Proof follows from Lemma 1 in Section 3.

Example 1: for stuck-ON of transistor D shown in Figure 4, the set N_{1t}^f is $N_{1t}^f = \{\underline{x} \mid (A+B)C = 1\}$

which results in the following sets { 01100, 01101, 01110, 01111, 10100, 10101, 10110, 10111, 11100, 11101, 11110, 11111 }

The sets P_t^f and N_{2t}^f for faults in the p-part and n-part(2) can be derived in a similar manner.

Lemma 8: For a stuck-OPEN fault in transistor x_i, the set N_{1t}^f is given by
$N_{1t}^f = \{\underline{x} \mid h(\underline{x}\ , x_i) = 1\}$

Proof follows from Lemma 4 in Section 3.

Example 2: for stuck-OPEN of transistor D shown in Figure 4, the set N_{1t}^f is $N_{1t}^f = \{\underline{x} \mid (A+B)CE = 1\}$

which results in the following sets { 01101, 01111, 10101, 10111, 11101, 11111 }

The sets P_t^f and N_{2t}^f for faults in the p-part and n-part(2) can be derived in a similar manner.

6 Conclusions

Manifestations of faults in BiCMOS were compared with CMOS and TTL to bring out the testability differences. In addition to sequential behavior observed in CMOS devices, BiCMOS devices also exhibit delay faults. Some of the stuck-ON faults can be detected by observing voltage level, however, power supply current (I_{DDQ}) monitoring would definitely detect the fault. A comparison of the faulty behaviors of the three different families, namely, TTL, CMOS and BiCMOS was presented to bring out the testability differences between the three logic families. A pattern classification scheme was shown for BiCMOS gates under different faults and were represented using Venn diagrams. A methodology for generation of test sets in BiCMOS circuits using the above scheme was presented. The test sets obtained at switch level now can be used to generate test vectors that can be applied at the primary inputs of the circuit to detect these faults.

References

[1] A. R. Alvarez, *BiCMOS Technology and Applications*, Kluwer Academic Publishers, 1989.

[2] M. E. Levitt, K. Roy and J. A. Abraham, *'BiCMOS fault models: Is stuck-at adequate?'*, Proc. ICCD., pp. 294-297, Sep. 1990.

[3] S. M. Menon, Y. K. Malaiya and A. P. Jayasumana, *'Behavior of Faulty Single BJT BiCMOS Logic Gates'*, Proc. of the 10th IEEE VLSI Test Symposium, pp. 315-320, April 1992.

[4] S. M. Menon, Y. K. Malaiya and A. P. Jayasumana, *'Behavior of Faulty Double BJT BiCMOS Logic Gates'*, Proc. of the 4th NASA Symposium on VLSI Design, pp. 8.4.1-8.4.12, October 1992.

[5] A. E. Salama and M. I. Elmasry, *'Testing and Design for Testability of BiCMOS Logic Circuits'*, Proc. of the 10th IEEE VLSI Test Symposium, pp. 217-222, April 1992.

[6] S. M. Menon, A. P. Jayasumana and Y. K. Malaiya *'A Detailed Analysis of faults in Single and Double BJT BiCMOS Logic Gates'*, Technical Report CS-93-122, Dept. of Electrical Engineering/Computer Science, Colorado State University, Sept. 1993.

[7] D. Al-Khalili, C. Rozon and B. Stewart, *'Testability Analysis and Fault Modeling of BiCMOS Circuits'*, Jrnl. of Electronic Testing Theory and Applications (JETTA), pp. 207-217, August 1992.

[8] M. Favalli, M. Dalpasso, P. Olivo and B. Ricco, *'Analysis of Steady State Detection of Resistive Bridging Faults in BiCMOS Digital ICs'*, Proc. of the IEEE Intl. Test Conf., pp. 466-475, 1992.

[9] S. M. Menon, Y. K. Malaiya and A. P. Jayasumana, *'Bridging Faults in BiCMOS Circuits'*, Proc. of the 5th NASA Symposium on VLSI Design, pp. 7.1.1-7.1.10, Nov. 1993.

[10] S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, *'Test Generation for BiCMOS Circuits'*, Proc. IEEE Intl. Symposium on Circuits & Systems (ISCAS '93), pp. 1987-1990, May 1993.

[11] S. M. Menon, A. P. Jayasumana and Y. K. Malaiya, *'Testable Design for BiCMOS Stuck-Open Fault Detection'*, Proc. IEEE VLSI Test Symp., pp. 296-302, April 1993.

[12] Y. K. Malaiya and S. Y. H. Su, *'A New Fault Model and Testing Technique for CMOS Devices'*, Proc. Intl. Test Conference, 1982.

[13] Y. K. Malaiya, A. P. Jayasumana, Q. Tong and S. M. Menon, *'Enhancement of Resolution in Supply Current Based Testing for Large ICs'*, Proc. of IEEE VLSI Test Symposium, pp. 291-296, April 1991.