Department of Computer Science

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Sankaran M. Menon, Yashwant K. Malaiya,
Anura P. Jayasumana, Carol Q. Tong

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The Effect of Built-In Current Sensors (BICS) on Operational and Test Performance*

Sankaran M. Menon Yashwant K. Malaiya‡
Anura P. Jayasumana Carol Q. Tong
Dept. of Electrical Engineering, ‡Dept. of Computer Science
Colorado State University
Ft. Collins, CO 80523

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Abstract

Effects of built-in current sensors on I_{DDQ} measurement as well as on the performance of circuit under test are considered. Most of the Built-In Current Sensor designs transform the ground terminal of the circuit under test to a virtual ground. This causes increase in both propagation delay as well as I_{DDQ} sampling time with the increase in the number of gates, affecting both test as well as operational performance. The effect that current sensor has on the operational and test performance are considered. Circuit partitioning may be used for overcoming the effects of BICS on I_{DDQ} measurements as well as on the performance of the circuit under test.

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1 Introduction

The use of leakage current measurement to detect faults in CMOS ICs has been under consideration for a number of years [1]. Recent studies on leakage current based testing techniques [2, 3, 4], have concluded that it is necessary to include I_{DDQ} monitoring to obtain highly reliable CMOS ICs. The data presented for four sample CMOS ICs showed that the defect detection increased between 60% to 180% when I_{DDQ} monitoring is added to a functional test set [2]. I_{DDQ} testing was demonstrated to reduce line fallout after 99.6% stuck-at fault testing failed to achieve desired quality goals [5].

I_{DDQ} testing is performed using either an external or a Built-In Current Sensor(BICS). Implementation of built-in current sensors has received a lot of interest in the recent years. Built-in current sensors have an advantage over external sensors in terms of test speed. This paper presents some of the drawbacks of BICS in terms of increase in propagation time (t_{pd}) as well as settling time (t_s) affecting both the operational as well as test performances.

2 Background

There are several reasons for using I_{DDQ} monitoring for testing of ICs [6], [7]. Traditional IC testing techniques are not effective in detecting a number of failure modes in CMOS ICs. In general, faults such as gate oxide shorts [6], certain bridging faults, certain open faults, stuck-on faults, punch-through faults, operation induced faults, parasitic devices, pn junction leakage, and abnormally high contact resistance, may not manifest as logic faults and therefore will not be detected by traditional tests which monitor the output logic levels.

In functional testing, the site of a fault has to be excited and the effect of the fault has to be propagated to the output. In I_{DDQ} testing, the propagation of the effect is automatic. Further, it can provide transistor level resolution as opposed to gate level resolution. Off chip current testing has proved to be very efficient for circuits like static RAMs [8].

Stuck-on faults in CMOS circuits cannot be detected using traditional functional fault testing techniques. Test generation for detection of such faults, when I_{DDQ} testing is used, is considered in [9]. The different types of current probes in use are examined in [10], and a probe circuit has been proposed which allows a system to perform dynamic I_{DDQ} tests as an integral part of the functional testing of a CMOS device.

Built-in current sensing techniques have been proposed to overcome the disadvantages of existing off-chip current testing techniques. Current sensors have been proposed and implemented using CMOS technology, some capable of detecting currents as small as 2μa at 1MHz clock frequency [3], [6]. In BIC

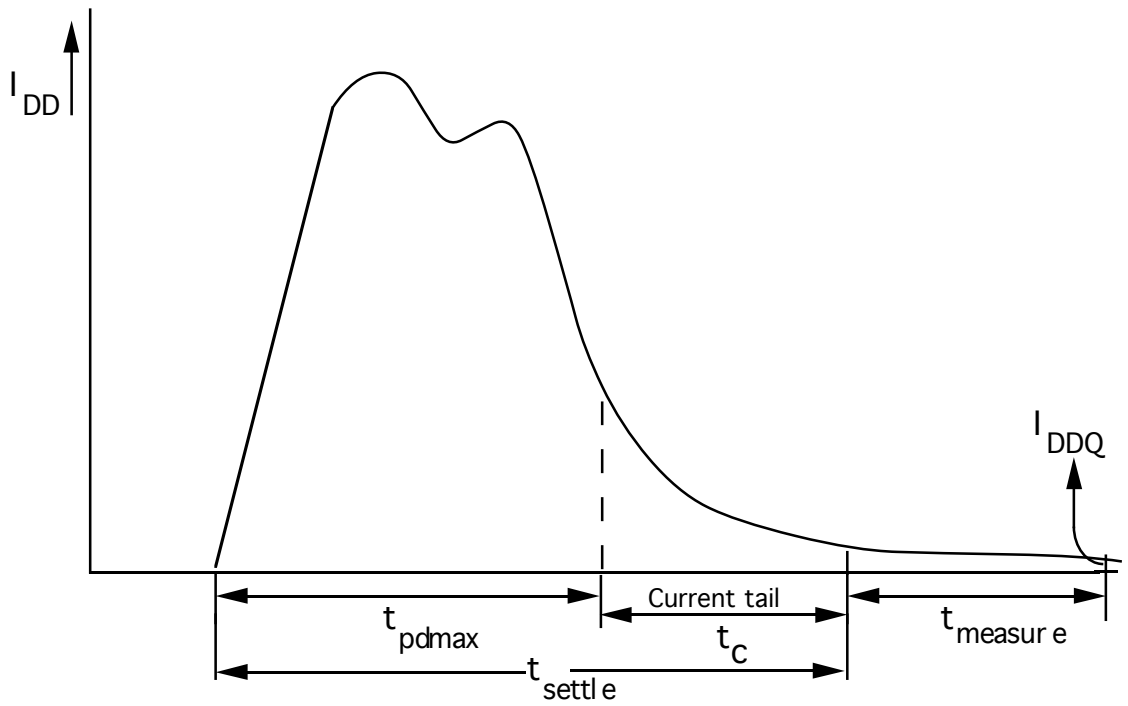

Figure 1: Plot illustrating I_{DD} vs. Time for a CMOS circuit

testing, an IC is implemented using a number of modules and each module is connected to the power supply through a current sensor.

3 Built-In Current Sensors

The simplest current sensor can be built with either a resistive [3, 4] or a capacitive [11] element along with a voltage comparator. Various current sensors have been proposed [3, 10, 11, 12]. The BICS proposed by Maly et. al. [3, 4] is based on a non-linear resistance placed in the power supply current path. The exponential I-V characteristics exhibited by the non-linear resistance causes distinguishable voltage drop for wide range of currents. The output of the current sensor distinguishes between the normal and abnormal quiescent currents by comparing the voltage drops with a reference voltage.

One of the current sensor circuits proposed by Rubio et. al. [11] uses a capacitor instead of the non-linear resistance. Several schemes for current measurement are given in [10]. A circuit for built-in current testing presented in [12] measures the integral of the current during a certain time interval. The measured value of the current is used to decide if the circuit under test is fault-free or not.

In almost all of the BICS designs, the circuit under test is connected in series with the built-in current

sensors in a manner that the power supply ground terminal is connected to the BICS input. The bypass circuit generally is made up of an nMOS transistor which provides a path for the ground terminal of the circuit under test to the physical ground, under normal operation. In the BICS proposed by [3, 4], the bypass circuit is formed by an nMOS transistor and the base to emitter junction of a bipolar transistor. This results in the ground terminal of the CUT to be virtual ground.

4 Dependence of I_{DDQ} Testing on Circuit Size

When the circuit size is small, distinguishing the difference between normal and faulty I_{DDQ} values is not difficult. When the circuit size becomes large, it becomes hard to detect a fault using I_{DDQ} monitoring as the distinction between normal and faulty current becomes difficult. Furthermore, the larger the circuit size, more significant will be the effect of BICS on the operation speed and the test speed of the circuit. Below, we describe several factors regarding the effect of BICS on circuit operation and testing. The solution to this problem will be to partition the device under test into smaller modules. Each of the partition will have its own current sensor.

4.1 Difference between Normal & Faulty I_{DDQ} values

A statistical characterization of faulty and fault-free I_{DDQ} distributions is presented in [13, 14]. The distinction between the distributions of normal and faulty I_{DDQ} is easy if the distributions are well separated. If the number of gates in a circuit is small, then the distributions between normal and faulty I_{DDQ} are well separated and thus the fault is detectable. As the number of gates in a circuit increases, the spread of the current distributions, both faulty and fault-free, increase making the distributions overlap. The spreading of the distributions occur due to the variations in circuit parameters over different gates in an IC. To use I_{DDQ} testing in the presence of this, the size of each module connected to a BICS has to be such that the faulty and normal distributions within each module can be distinguished. An upper bound of maximum n, denoted by n_b is given as [13, 14];

$$n_b = \left(\frac{\mu_{if}}{6\sigma_{iADDQ}}\right)^2 \tag{1}$$

where n is the number of cells covered by a current sensor. Hence, the device can be partitioned into modules whose sizes will not exceed n_b, and all the modules will have approximately the same number of cells. The above criterion ensures that the distributions of the normal and faulty I_{DDQ} are separated and distinguishable.

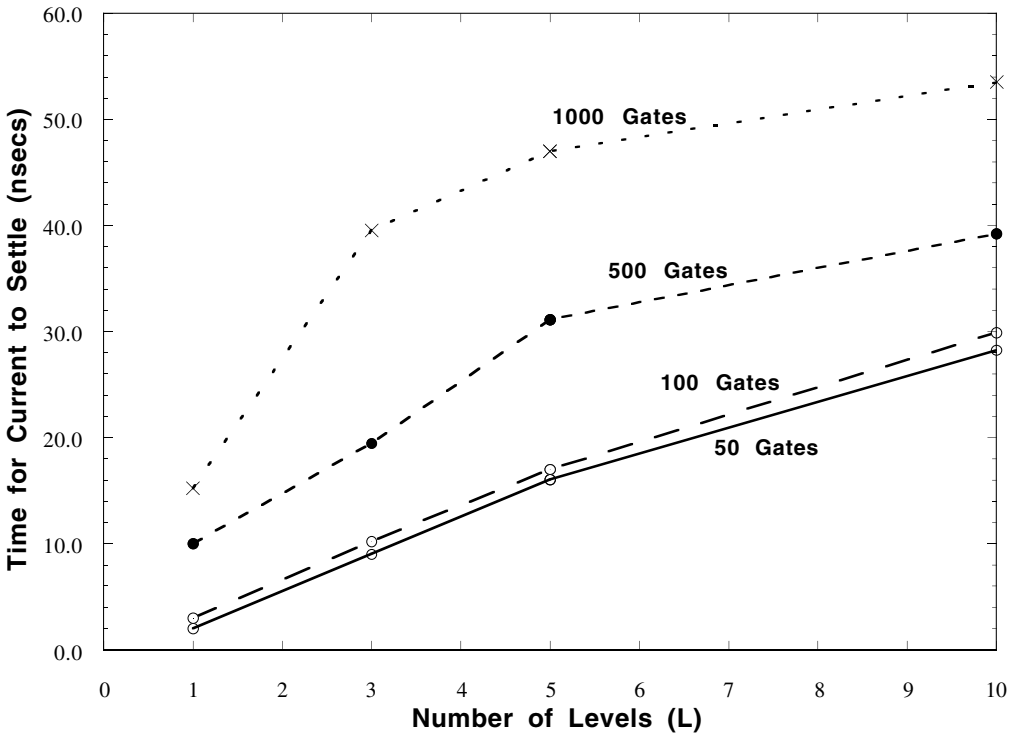

Figure 2: I_{DDQ} settling time vs. Number of Levels for various gate counts

4.2 Effects of BICS on Test Speed

For I_{DDQ} monitoring, the measurement of the supply current has to be performed by the current sensor after the initial transients have died down. Figure 1 shows a plot of I_{DD} vs. Time for a CMOS circuit. t_{pdmax} is caused due to the initial transients in the supply current due to switching in the various gates of the CMOS circuit. It takes certain amount of time (t_c) for the current tail to end, i.e., the current to settle to an almost constant value of the order of pico or nano amperes in a fault-free CMOS circuit. In a faulty CMOS circuit, the value of I_{DDQ} can be a few orders of magnitude greater than the fault-free I_{DDQ} value. The total time taken for the current to settle (t_s) is ($t_{pdmax} + t_c$).

Inverter chain of 1-level consisting of 5 inverters was simulated using SPICE, to obtain propagation delay (t_{pd}) and current tail (t_c). For I_{DDQ} monitoring, the sampling of the supply current can be done any time after the current tail has reached the almost fixed very low value of current in fault-free CMOS circuit. If the CMOS circuit is faulty, then the current at this time would be elevated and hence the BICS would be able to detect the fault. This results in a settling time of $t_{settle} = t_{pdmax} + t_c$.

CMOS circuits of different levels (1,3, 5 and 10 levels) were chosen for simulation with BICS (Built-in Current Sensor) to determine the time for current to settle. The number of levels indicate the number of gates connected in series with one another. For example, simulation for 5 levels totaling 500 gates has

Table 1: I_{DDQ} settling time vs. # of levels.

# of levels	**Total Number of Gates**							
	50 t_p (ns)	50 t_s (ns)	100 t_p (ns)	100 t_s (ns)	500 t_p (ns)	500 t_s (ns)	1000 t_p (ns)	1000 t_s (ns)
1-Lv(BICS)	1.15	2.0	1.41	3.0	4.22	10.01	13.46	15.23
1-Lv(No BICS)	0.66	0.6	0.66	0.6	0.66	0.6	0.66	0.6
3-Lv(BICS)	6.6	9.02	7.22	10.21	11.57	19.46	16.4	39.56
3-Lv(No BICS)	4.04	7.8	4.04	7.8	4.04	7.8	4.04	7.8
5-Lv(BICS)	11.51	16.06	11.76	17.0	16.71	31.12	21.42	47.0
5-Lv(No BICS)	7.56	10.8	7.56	10.8	7.56	10.8	7.56	10.8
10-Lv(BICS)	23.8	28.26	24.19	29.92	28.19	39.21	32.62	53.5
10-Lv(No BICS)	16.4	21	16.4	21	16.4	21	16.4	21

5 gates connected in series with 100 such series of gates in parallel. It may be noted that when BICS is implemented, the transistor terminals (source or drain) in a CMOS circuit which otherwise would have been connected to ground is connected to the BICS. The transistor terminal (source or drain) capacitance (C) of all the transistors appears as one lumped capacitance at the input of the BICS. The larger the circuit under test (CUT), the larger the capacitance seen by the BICS. Figure 2 shows plots for I_{DDQ} settling time vs. number of levels for various gates of CMOS circuits. In practice, the current is sampled by the BICS only after all the transients due to switching have died down and the current has settled to a steady low current value [3]. The settling time shown in Figure 2 shows the time when the current has settled to within 5% of the steady low current value for sampling by the BICS. For a circuit with a given number of gates, the settling time increases with the increasing number of levels. For example, for a circuit with 100 gates, the settling time for 3 levels is 10.21 ns and the settling time for 5 levels is 17 ns. The settling time thus has two components, one due to the propagation delay, and the other due to the capacitance at the node to which the current sensor is connected. Thus the larger the circuit that is covered by a current monitor, the longer the second component of the transient time will be. Another advantage of partitioning is the reduction of this component of settling time due to the total capacitance.

4.3 Effects of BICS on Circuit Performance

The bypass circuit of the BICS offers a finite resistance ($R^{'}$) which effectively appears in series with the circuit under test (CUT). This may not cause a significant problem under test conditions. However, under normal operation, the resistance of the BICS appears in series with the CUT and causes an IR voltage

drop across the BICS. The voltage drop in the BICS causes the effective ground potential of the CUT to be higher than the physical ground, especially during the transitions, thus slowing down the circuit operation.

The propagation delay (t_{pd}) component at the output of different levels (1, 3, 5 and 10 levels) for circuit with varying number of gates with implementation of BICS and without implementation of BICS is shown in Figure 3. The propagation delay (t_{pd}) for the different levels (1, 3, 5 and 10 levels) remains fixed with increasing number of gates in a given circuit for a certain fixed level, when BICS is not implemented. For example, the propagation delay (t_{pd}) for 1-level, 3-level, 5-level and 10-level (shown dotted in Figure 3) are 0.66ns, 4.04ns, 7.58ns and 16.4ns respectively even with increasing number of gates (n) for the case without BICS.

The propagation delay (t_{pd}) increases with increasing number of gates as the capacitance seen by BICS increases with increasing number of gates (transistors). Table 1 summarizes the settling time (t_{settle}) and propagation delay (t_{pd}) for 1, 3, 5 and 10-levels with increasing number of gates up to 1000 gates, with and without BICS implementation. In order to evaluate only the effect of current sensor, we have used an ideal source. Under this condition, the t_{pd} and t_s values do not change for a given level, when the number of gates are increased in the absence of BICS. Therefore the values of t_s given in Table 1 for the case of No BICS with 500 gates and 1000 gates are included without actually doing the simulations. The settling time (t_{settle}) of current for a given CMOS circuit with BICS is a function of the following:

$$t_{settle} = f(T_{pd}, R^{'}, C, D_{pd}, t_r/t_f)$$

where T_{pd} = the maximum end to end propagation delay in a CMOS circuit,
D_{pd} = Distribution of propagation delays amongst the various levels of the circuit.
C = total capacitance of the V_{DD} or Ground rail of CUT connected to BICS,
$R^{'}$ = denotes the effect due to BICS resistance,
t_r and t_f = rise-time and fall-time of the gate switching towards the end.

With the above results, the partitioning of a given circuit becomes very critical as the capacitance offered at the input of BICS also needs to be considered, in addition to the voltage drop across the BICS and resolution of the BIC sensor. Partitioning the circuit under test into smaller modules reduce the amount of capacitance seen by the BICS which in turn reduces the settling time for I_{DDQ} measurement. Partitioning reduces the settling time which in turn helps in performing faster sampling of I_{DDQ} measurement. The effect of increase in settling time (t_s) with increasing number of gates for a given level due to the capacitance (C) is a problem for all BICS designs which rely on virtual ground.

The effect of the lumped capacitance (C) of the circuit and the non-linear resistance ($R^{'}$) of the BICS results in additional propagation delay of the CMOS circuit. This is a problem effecting the operational

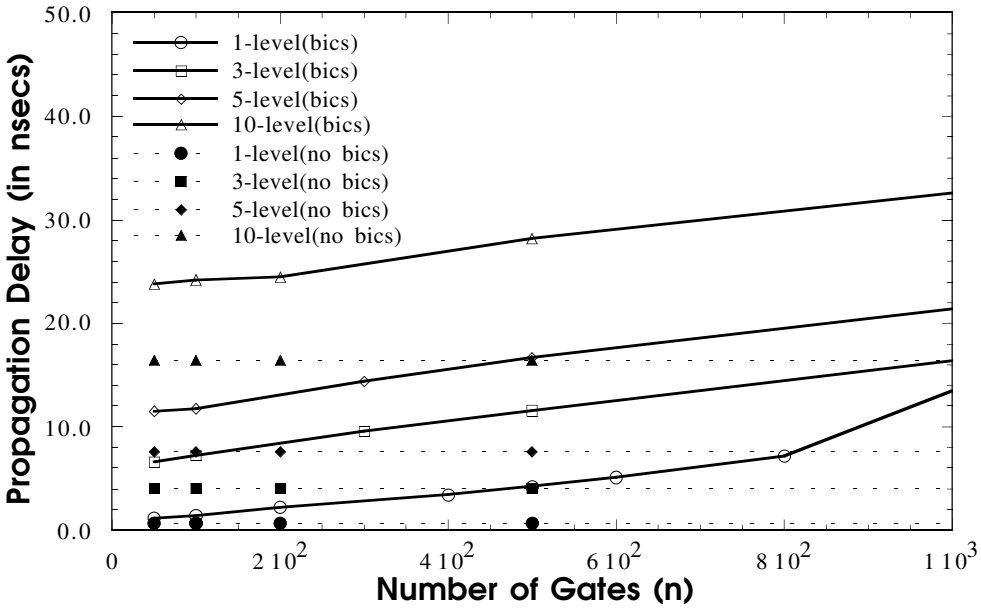

Figure 3: Propagation delay t_{pd} vs. Number of gates for different levels

performance of the circuit caused due to BICS. This can be avoided by providing a physical ground pin in addition to the virtual ground pin. This facilitates the ground pin to be connected to the ground terminal of the system and hence avoiding the propagation delay introduced in the circuit by the BICS. This scheme provides for off-line BICS, wherein whenever current sensing is required to be carried out, the BICS is introduced into the circuit by disabling the ground pin and making it a virtual ground. The BICS in this scheme is disabled by connecting the virtual ground terminal to the physical ground, thus avoiding the additional propagation delay introduced due to the capacitance (C). In this scheme, BICS is introduced only during test mode. The off-line BICS scheme suffers the disadvantage of switching the circuit into test and normal modes of operation, thus the inability to monitor the I_{DDQ} drawn by the circuit on-line.

Since each module or subcircuit has its own current sensor, it is impractical to observe the output of every current sensor. One solution to this problem is to propagate the outputs of all the sensors to one observable output pin which is designed solely for the signature extractor or information compression unit. This information compression unit maybe implemented simply by an OR gate. The outputs from all the current sensors are fed to the OR gate.

Figure 4 shows the circuit under test partitioned into n partitions with a BICS for each partition. Capacitor C is the lumped capacitance of the source terminal of all the transistors which other wise would have been connected to ground terminal if BICS is not implemented. The capacitance (C) plays

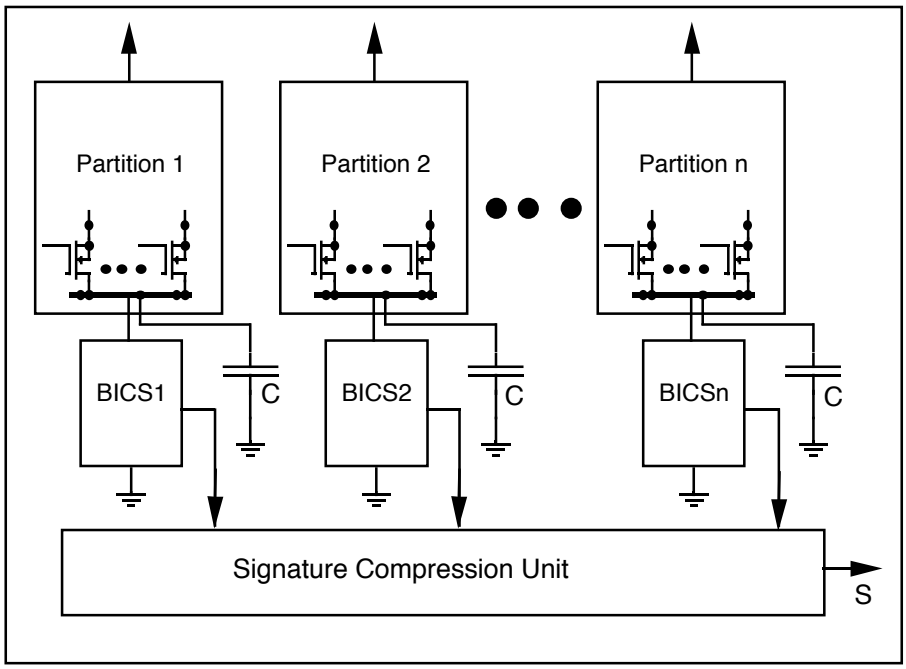

Figure 4: Partitioning and information compression

a crucial role in affecting both the operational and test performance when BICS is implemented [13, 14].

5 Conclusions

I_{DDQ} monitoring of large ICs requires larger test times and exhibits lower resolution between faulty and fault-free devices. Effect of BICS on I_{DDQ} measurement causing increased delay with increasing gates is presented. Effect on the performance of the circuit under test exhibiting increased delay with increasing gates is shown. Partitioning of large circuits as well as forcing the virtual ground to physical ground using an additional pin may help minimize the effects of BICS on the performance of circuit under test.

References

[1] Y.K. Malaiya and S. Y. H. Su, "A new fault model and testing technique for CMOS devices," *Proc. Int. Test Conf., pp. 25-34,* 1982.

[2] C.F. Hawkins, J. M. Soden, R.R. Fritzemeier and L. K. Horning, "Quiescent power supply current measurement for CMOS IC defect detection," *IEEE Trans. Industrial Electronics, pp. 211-218,* May 1989.

[3] W. Maly et. al., "Built in Current Testing," *Research Report No. CMUCAD-88-27*, Carnegie Mellon University.

[4] W. Maly and P. Nigh, "Built in Current Testing - Feasibility Study," *Proc. ICCAD, pp. 340-343*, 1988.

[5] R. Perry, "I_{DDQ} testing in CMOS digital ASIC's - Putting it all together," *Proc. Int. Test Conf., pp. 151-157,* 1992.

[6] K. Baker and B. Verhelst, "IDDQ testing because 'Zero Defects isn't Enough: A Philips Perspective," *Proc. IEEE Int. Test Conf., pp. 253-254,* 1990.

[7] S. McEuen, "IDDq Benefits", *Proc. IEEE VLSI Test Symp., pp. 285-290,* 1991.

[8] R. Meershoek, B. Verhelst, R. McInerney and L. Thijssen, "Functional IDDQ Testing on a Static RAM," *Proc. IEEE Int. Test Conf., pp. 929-937,* 1990.

[9] Y. K. Malaiya, "Testing stuck-on faults in CMOS integrated circuits," *Proc. Int. Conf. on Computer Aided Design, pp. 248-250,* 1984.

[10] M. Keating and D. Meyer, "A new approach to dynamic IDD testing," *Proc. Int. Test Conf., pp. 316-321,* 1987.

[11] A. Rubio, J. Figueras and J. Segura, "Quiescent Current Sensor Circuits in Digital VLSI CMOS Testing," *Electronics Letters, pp. 1204-1206,* July 1990.

[12] Y. Miura and K. Kinoshita, "Circuit design for built-in current testing," *Proc. Int. Test Conf., pp. 873-881,* 1992.

[13] Y. K. Malaiya, A. P. Jayasumana, Q. Tong and S. M. Menon, "Enhancement of resolution in supply current based testing for large ICs," *Proceedings of IEEE VLSI Test Symposium, pp. 291-296,* 1991.

[14] Y. K. Malaiya, A. P. Jayasumana, Q. Tong and S. M. Menon, "Resolution Enhancement in I_{DDQ} based testing for large ICs," *Tech. Rep. CS-92-143, Dept. of Computer Science, Colorado State University, Fort Collins CO.,* 1992.