# Department of Computer Science

## A Detailed Analysis on the Manifestations of Faults in Single and Double BJT BiCMOS Logic Gates

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Technical Report CS-93-122

September 20, 1993

# Colorado State University

# A Detailed Analysis on the Manifestations of Faults in Single and Double BJT BiCMOS Logic Gates*

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## Abstract

Combining the inherent advantages of Bipolar and CMOS, BiCMOS is emerging as a major technology for high speed, high performance, digital and mixed signal applications. Logic Behavior of Single and Double BJT BiCMOS devices under transistor level shorts and opens is examined. In addition to sequential behavior, some stuck-OPEN faults exhibit delay faults. While most stuck-ON faults can be detected by logic level testing, some of them can only be detected by monitoring the power supply current ($I_{DDQ}$ monitoring). A stuck-OPEN fault manifesting as enhanced dynamic $I_{DD}$ current is shown in double BJT BiCMOS devices. The faulty behavior of Single and Double BJT BiCMOS NAND and NOR, CMOS NAND and NOR, TTL NAND and NOR are presented. The faulty behavior of Bipolar (TTL) and CMOS logic families is compared with BiCMOS. Testability of both Single and Double BJT BiCMOS devices are discussed.

*This research was supported by a SDIO/IST funded project monitored by ONR.

# 1 Introduction

BiCMOS technology, which combines the advantages of CMOS and bipolar, is emerging as a major technology for many high performance digital and mixed signal applications. The main advantages of CMOS technology over bipolar are lower power dissipation and higher packing density. Bipolar technology offers better output current drive, switching speed, I/O speed and analog capability. Combining the advantages of bipolar and CMOS, BiCMOS offers the following advantages [1]; improved speed over CMOS, lower power dissipation compared to bipolar, flexibility in I/O (TTL, ECL, CMOS compatibility), high performance analog capability and latch up immunity. Compared to the CMOS counterparts, BiCMOS circuits can be faster by a factor of upto two for the same level of technology. Access times of less than 10nS have been reported for 0.8 $\mu$m BiCMOS ECL input/output 256K and 1M-bit SRAMs [2]. 100K gate arrays operating at 100MHz clock rates have also been reported [2]. BiCMOS is even being considered for high performance microprocessors and dynamic RAMs, and it is felt that it will be one of the main technologies to drive almost all functions in the decade ahead [3].

Most of the defects and failures in present day integrated circuits can be abstracted to shorts and opens in the interconnects and degradation of devices [4]. Transistor level shorts and opens model many of the physical failures and defects in ICs [5]. A study by Gailiay [6] on 4-bit MOS microprocessor chips revealed that many of the faults were shorts and opens at the transistor level. Analysis of faults in elementary static storage elements suggest that transistor level testing provides a higher coverage of faults compared to that at the gate level [7]. Thus, it is necessary to study the effects of failures at the transistor level and develop accurate fault models at this level [5].

The major fault models at transistor level are stuck-at faults, and shorts and opens of transistors and interconnects [8]. It has been shown [9, 10, 11, 12, 13] that the stuck-at model does not cover many of the manufacturing defects in BiCMOS devices and that most open faults manifest themselves as delay faults. Analysis on the effects of bridging faults in BiCMOS is given in [14, 15]. A merged BiCMOS circuit configuration to improve BiCMOS gate performance at low supply voltage is presented in [16]. Reference [13] presents testability analysis and fault modeling of BiCMOS circuits in which the behavior of BiCMOS under faults is compared with CMOS. The most common type of BiCMOS circuits employ bipolar transistors to perform the function of driving output loads and CMOS to perform logic functions. In this paper, we briefly review the operation of a single BJT (S-BJT) and double BJT (D-BJT) BiCMOS NAND device. Since BiCMOS technology combines the advantages of both CMOS and bipolar, we compare the faulty behavior of BiCMOS with CMOS and bipolar (TTL). A

Figure 1: An S-BJT BiCMOS NAND.

stuck-open fault manifesting in enhanced dynamic $I_{DD}$ is presented which can be detected using $I_{DDQ}$ monitoring. Testability aspects of BiCMOS devices are also presented.

This paper is organized as follows. The operation of basic S-BJT and D-BJT BiCMOS NAND devices are described in section 2. Section 3 deals with delay measurements. Sections 4 and 5 deal with the analysis of physical failures in S-BJT and D-BJT BiCMOS devices respectively, where the logic behavior of BiCMOS devices in both the configurations are examined under different faults. Analysis of physical failures in BiCMOS NOR, CMOS (NAND & NOR) and TTL (NAND & NOR) devices are presented in section 6. Comparison of the three logic families (TTL, CMOS and BiCMOS) are done in section 7. Section 8 deals with testability of BiCMOS devices. Finally, conclusions drawn from the study are given in section 9.

# 2 BiCMOS Devices

BiCMOS circuits employ one or two Bipolar Junction Transistors (BJTs) to perform the function of driving output loads and CMOS to perform logic functions. In this section, the operation of S-BJT and D-BJT NAND devices and its logic levels are presented.

## 2.1 S-BJT BiCMOS device

A Single BJT BiCMOS NAND realization is shown in Figure 1. The functioning of the BiCMOS NAND can be explained by first applying logic '0' to one or both of the inputs which would cause at least one P-device to be ON and at least one N-device in each serial

Figure 2: A general S-BJT BiCMOS device

N-pairs to be OFF. With the P-devices ($P_1$ and/or $P_2$) ON, the base of the bipolar NPN transistor would be about 5V supplying base current and turning ON the bipolar transistor ($Q_1$) providing logic '1' at the output. With either of the inputs being at logic '0' and the other input at logic '1' would still cause either of the parallel connected P-devices to be ON and either of the series connected N-devices to be OFF. This would still supply base current to the bipolar transistor causing logic '1' at the output. With both the inputs at logic '1', the P-devices ($P_1$ and $P_2$) would be turned OFF, and the N-devices $N_1$, $N_2$, $N_3$ and $N_4$ would be turned ON causing a conduction path from output node to ground. This will cause the output to be a logic '0'. Thus the circuit realizes the NAND function. Block diagram of a general S-BJT BiCMOS device is shown in Figure 2. An S-BJT BiCMOS gate consists of CMOS p- and n-parts to perform logic function, and a BJT and a pull-down n-part for driving the output node.

S-BJT BiCMOS devices do not have the full $V_{DD}$ to Ground logic swing of CMOS devices. The output High voltage ($V_{OH}$) is limited to $V_{DD}$-$V_{BE(Q1)}$. However, output Low voltage ($V_{OL}$) is ≈0V. The DC Voltage transfer characteristics shown in Figure 3 of a BiCMOS inverter was examined to determine the logic levels [12]. $V_{ILmax}$ and $V_{IHmin}$ were determined to be 1.5V and 1.9V respectively, by finding the $\frac{dV_{out}}{dV_{in}}$ = -1 points [17, 18] on the voltage characteristics. It can be seen from Figure 3 that $V_{OHmax}$ is 4.4V ($V_{DD}$-$V_{BE(Q1)}$) and $V_{OLmin}$ is ≈0V. The logic levels for BiCMOS are 0 to 1.5V for logic level '0' and 1.9V to 4.4V for logic level '1' [12]. Any voltage between 1.5V and 1.9V is considered indeterminate. The device characteristics given for Fujitsu BiCMOS gate array devices [19] are $V_{IHmin}$=2V, $V_{OHmin}$=2.4V, $V_{ILmax}$=0.8V

Figure 4: DC Voltage transfer characteristics of a CMOS Inverter.

Figure 5: A D-BJT BiCMOS NAND.

and $V_{OLmax}$=0.5V. The DC Voltage transfer characteristics of a CMOS inverter is shown in Figure 4, for comparison. $V_{ILmax}$ and $V_{IHmin}$ for a CMOS inverter were determined to be 2.4V and 2.9V respectively. CMOS devices exhibit rail-to-rail logic swing resulting in $V_{OHmax}$ of $\approx$5V and $V_{OLmin}$ of $\approx$0V.

## 2.2 D-BJT BiCMOS device

A Double BJT BiCMOS NAND realization is shown in Figure 5. The functioning of the BiCMOS NAND can be explained by first applying logic '0' to one or both of the inputs which would cause at least one P-device to be ON and at least one N-device in each serial N-pairs to be OFF. With at least one N-device in each serial N-pairs being OFF, no current is supplied to the base of $Q_2$ resulting in transistor $Q_2$ being OFF. With the P-devices ($P_1$ and/or $P_2$) ON, the base of the bipolar NPN ($Q_1$) transistor would be about 5V supplying base current and turning ON the bipolar transistor ($Q_1$) providing logic '1' at the output. Either of the inputs being at logic '0' and the other input at logic '1' would still cause either of the parallel connected P-devices to be ON and either of the series connected N-devices to be OFF. This would still supply base current to the bipolar transistor $Q_1$ causing logic '1' at the output. With both the inputs at logic '1', the P-devices ($P_1$ and $P_2$) would be turned OFF, and the N-devices $N_1$, $N_2$, $N_3$ and $N_4$ would be turned ON, supplying base current to $Q_2$ which discharges the load. Transistor $N_1$ and $N_2$ draw current from the base of $Q_1$ thus

Figure 6: A general D-BJT BiCMOS device.

rapidly turning this device OFF. This will cause the output to be a logic '0'. Thus the circuit realizes the NAND function. It may be noted that during output High to Low transition, transistor $N_5$ turns OFF as a result of transistors $N_1$ and $N_2$ discharging $Q_1$ base, causing the gate of $N_5$ to be low [20], this results in all the current through $N_3$ and $N_4$ to be provided as base current to transistor $Q_2$. During output Low to High transition, transistor $N_5$ turns ON to discharge the base of $Q_2$ quickly to speed up the transition. It may also be noted that the static power consumption of the circuit is negligible neglecting reverse biased leakage currents. Block diagram of a general D-BJT BiCMOS device is shown in Figure 6. A D-BJT BiCMOS gate consists of CMOS p- and n-parts to perform logic function, and two output BJTs for driving the output node.

D-BJT BiCMOS devices do not have the full $V_{DD}$ to Ground logic swing of CMOS devices. The output High voltage ($V_{OH}$) is limited to $V_{DD}$-$V_{BE(Q1)}$ and output Low voltage ($V_{OL}$) is limited to $Gnd$+$V_{BE(Q2)}$. The DC Voltage transfer characteristics shown in Figure 7 of a D-BJT BiCMOS inverter was examined to determine the logic levels [12]. $V_{ILmax}$ and $V_{IHmin}$ were determined to be 2.2V and 2.7V respectively, by finding the $\frac{dV_{out}}{dV_{in}}$ = -1 points [17, 18] on the voltage characteristics. It can be seen from Figure 7 that $V_{OHmax}$ is ≈4.4V ($V_{DD}$-$V_{BE(Q1)}$) and $V_{OLmin}$ is ≈0.6V ($Gnd$+$V_{BE(Q2)}$). The logic levels for BiCMOS are 0.6V to 2.2V for logic level '0' and 2.7V to 4.4V for logic level '1' [12]. Any voltage between 2.2V and 2.7V is considered indeterminate. The device characteristics given for Fujitsu BiCMOS gate array

Figure 7: DC Voltage transfer characteristics of an D-BJT BiCMOS Inverter.

devices [19] are $V_{IHmin}$=2V, $V_{OHmin}$=2.4V, $V_{ILmax}$=0.8V and $V_{OLmax}$=0.5V. The DC Voltage transfer characteristics of a CMOS inverter is shown in Figure 4, for comparison. $V_{ILmax}$ and $V_{IHmin}$ were determined to be 2.4V and 2.9V respectively. CMOS devices exhibit rail-to-rail logic swing resulting in $V_{OHmax}$ of $\approx$5V and $V_{OLmin}$ of $\approx$0V.

# 3 Delay Measurements in BiCMOS Devices

In FCMOS (Fully CMOS) circuits, gate delay $t_{LH}(t_{HL})$ is normally defined as the delay from the time input to a gate crosses $0.5V_{DD}$ to the time when the falling(rising) output crosses $0.5V_{DD}$ [21]. Since the switching threshold in the voltage transfer characteristics of a CMOS inverter is approximately $\frac{V_{DD}}{2}$, this definition is fairly valid. However, in BiCMOS devices, the switching threshold need not be very close to $\frac{V_{DD}}{2}$ as seen in the voltage characteristics of S-BJT BiCMOS devices [12]. Hence, the voltage characteristics need to be carefully analyzed to determine the switching threshold for the purpose of delay measurements.

Switching threshold is determined by plotting $V_o$=$V_{in}$ and identifying the intersection of this line on the voltage characteristics [22]. The switching threshold for the gates used in this study is determined from the DC voltage transfer characteristics to be 1.9V for S-BJT BiCMOS, 2.5V for D-BJT BiCMOS and 2.65V for CMOS [12].

If delay measurement for BiCMOS devices is done similar to that for CMOS devices, i.e., from the time input to a gate crosses $0.5V_{DD}$ to the time when the falling(rising) output crosses $0.5V_{DD}$. For falling outputs, the output logic level cannot be termed as '0' logic level at $0.5V_{DD}$. This is because 2.5V is considered as logic '1' level for S-BJT BiCMOS devices

[12]. Under delay faults if the output level remains very close to 2.5V, the logic level has not crossed the switching threshold and cannot be termed as delay fault. Now, if $0.5V_{DD}$ cannot be used as the point for delay measurement, a question arises as to which point is to be used for delay measurement.

For determining logic levels, $V_{ILmax}$ and $V_{IHmin}$ were obtained by finding the $\frac{dV_{out}}{dV_{in}}$ = -1 points. The switching threshold of the device has to be in between $V_{ILmax}$ and $V_{IHmin}$ and this has to be determined by finding the intersection of $V_o$=$V_{in}$ on the voltage transfer characteristics.

Some delay faults in BiCMOS devices do not necessarily cross the logic threshold as shown later in sections 4.2 and 5.2, depending on fan-out, pulse-width etc., and such faults cannot be termed as delay faults. They can be termed as stuck-at faults for all practical purposes, as logic monitoring exhibits stuck-at behavior. Even though some High to Low transition delay faults result in the output level reaching Undefined level, which could cause the gate connected to the output of this device to get switched as soon as the logic level reaches the switching threshold. Hence, it is more accurate to perform delay measurements from the level at which switching takes place (switching threshold). In this study, we perform delay measurements between switching thresholds which for S-BJT BiCMOS is determined to be 1.9V and for D-BJT BiCMOS is determined to be 2.5V.

# 4 Analysis of Physical Failures in S-BJT BiCMOS Devices

In this section, the response of the S-BJT BiCMOS NAND is evaluated for hard failures of the bipolar and MOS transistors. Possible failures considered are stuck-ONs, and stuck-OPENs of transistors. The output of the BiCMOS gate is examined by simulating one failure at a time for all possible stuck-ON and stuck-OPEN failures of all the transistors. Stuck-ON faults and stuck-OPEN faults were simulated by turning ON and turning OFF the corresponding transistors. Open (OP) in bipolar transistor terminals (emitter, base & collector) were simulated by connecting a resistance of R>1M$\Omega$ in series with the respective node and short (SH) were simulated by connecting a hard short of R<0.01$\Omega$ between the respective terminals. The BiCMOS gate outputs obtained analytically have been compared with SPICE simulation outputs to ensure correctness.

The fault-free and faulty behavior (Stuck-ON and Short faults) of BiCMOS NAND are summarized in Table 1 and Stuck-OPEN faults are summarized in Table 2. The length and width of pMOS ($L_p$,$W_p$) and nMOS ($L_n$,$W_n$) transistors used for BiCMOS devices in this study are ($L_p$=1.5$\mu m$,$W_p$=30$\mu m$,$L_n$=1.5$\mu m$,$W_n$=26$\mu m$) similar to the values used in [9].

Figure 8: S-BJT BiCMOS NAND with CMOS inverter load and driver

Simultaneous current monitoring was performed during SPICE simulation and the observed $I_{DDQ}$ values are listed in the Tables along with the output logic levels. In Tables 1 and 2, the subscript represents the transistor number for the BiCMOS circuit shown in Figure 1 and superscript represents the type of hard failure under consideration where ON indicates stuck-ON failure and OP indicates stuck-OPEN failure. For example, $N_1^{ON}$ indicates transistor $N_1$ stuck-ON, $N_1^{OP}$ indicates transistor $N_1$ stuck-OPEN, $Q_{1c}^{OP}$ indicates transistor $Q_1$ collector open and $Q_{1ce}^{SH}$ indicates transistor collector to emitter short.

In order to make the analysis a true representative of circuit conditions, CMOS inverters were used to drive the BiCMOS device and CMOS inverters were used as loads to the BiCMOS device as shown in Figure 8. The dimensions of pMOS and nMOS transistors used as CMOS driver devices in this study are ($L_p$=5$\mu m$,$W_p$=60$\mu m$) and ($L_n$=5$\mu m$,$W_n$=20$\mu m$) respectively. The sizes for the CMOS load devices used are ($L_p$=5$\mu m$,$W_p$=40$\mu m$) and ($L_n$=5$\mu m$,$W_n$=15$\mu m$). To study the effects of output fan-out on BiCMOS devices, analysis was conducted with one CMOS load alone and also with an RC (Resistor Capacitor) load along with a CMOS load as shown in Figure 8. R=100$\Omega$ and C=1pF were chosen for this study and RC load referred to henceforth in this paper refers to the above values.

## 4.1 Stuck-ON faults in S-BJT BiCMOS NAND

Stuck-ON faults in S-BJT BiCMOS NAND generally result in a fault-free logic level, faulty logic level or indeterminate logic level. However, in all the cases, it results in enhanced $I_{DDQ}$.

Referring to the S-BJT BiCMOS NAND shown in Figure 1, for the physical failure $P_1^{ON}$, the device behaves similar to fault-free gate for all input vectors except for input vector '11'. Input vector '11' causes all the N-devices to be ON providing a conduction path from $V_{DD}$ to $V_{SS}$ (Gnd), resulting in enhanced $I_{DDQ}$. The current drawn by the device with this vector for the fault under consideration is $\approx$2mA instead of the normal $\approx$0.2$\mu$A. Current testing technique can be employed to detect this fault. A similar result is observed for transistor $P_2$

stuck-ON fault ($P_2^{ON}$). SPICE simulation indicates the output voltage level to be ≈1.16V, which is logic '0' level for S-BJT BiCMOS devices indicated as '0' in Table 1.

Transistor $N_1$ stuck-ON fault results in enhanced $I_{DDQ}$ for input vector '01'. SPICE simulation indicates output voltage to be ≈2.42V, which is logic '1' level for S-BJT BiCMOS devices. Similarly, enhanced $I_{DDQ}$ is observed for transistor $N_2$ stuck-ON fault with input vector '10'. SPICE simulation indicates the output voltage level to be ≈1.7V, which is an indeterminate ($I^*$) voltage level for BiCMOS devices. At a first glance, one would expect the output voltage level to be the same for $N_1^{ON}$ and $N_2^{ON}$. On careful analysis, it can be seen that the channel resistance will be different due to the non-linear characteristics of the nMOS transistor for the individual stuck-ON failures $N_1^{ON}$ and $N_2^{ON}$, leading to the different output voltage levels.

Stuck-ON failures of transistors $N_3$ and $N_4$ would result in enhanced $I_{DDQ}$ for input vectors 01 & 10 respectively. However, the fault-free and faulty output is logic '1' for input vectors 01, 10 and 11. Since fault-free and faulty logic level is the same, current testing alone can detect the failures. Transistor $Q_{1ce}^{SH}$ and $Q_{1bc}^{SH}$ shorts also result in enhanced $I_{DDQ}$ and cause a faulty output logic level '1' for input vector 11. Transistor $Q_{1be}^{SH}$ results in delay faults for output Low to High transitions as the base to emitter junction does not get forward biased and hence the transistor does not get turned ON. The Low to High transition Delay observed for transistor $Q_{1be}^{SH}$ short with RC output load is 2.08ns compared to the fault-free delay of 0.90ns.

Current testing can be very effective for testing failures which result in elevated $I_{DDQ}$ from a normal ≈0.2$\mu$A to enhanced ≈2mA, an increase by a factor of ≈$10^4$. Conventional logic testing cannot be used to detect stuck-ON failure $N_2^{ON}$ as the failure exhibits indeterminate output. However, current testing can detect the above stuck-ON failures. Since stuck-ON failures $P_1^{ON}$, $P_2^{ON}$, $N_1^{ON}$, $N_3^{ON}$ and $N_4^{ON}$ provide same logic level for faulty as well as fault-free operations, current testing alone can detect the failures. Conventional logic testing can detect the failures $Q_{1ce}^{SH}$ and $Q_{1bc}^{SH}$ as the logic output is different for fault-free and faulty operations, however, current testing would detect this failure mode. Delay fault caused by transistor $Q_{1be}^{SH}$ can be detected by delay test.

## 4.2 Stuck-OPEN faults in S-BJT BiCMOS NAND

Stuck-OPEN faults in S-BJT BiCMOS NAND result in either sequential behavior or delay faults.

Two faults in the S-BJT BiCMOS NAND exhibit sequential behavior ($Q_n$), similar to the behavior seen in CMOS circuits. Presence of the fault $P_1$ stuck-OPEN would result in

Table 1: Behavior of S-BJT BiCMOS NAND with Stuck-ON and Short faults between terminals for all transistors.

| **Single BJT BiCMOS NAND Stuck-ON and Short results** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | *ff* | $P_1^{ON}$ | $P_2^{ON}$ | $N_1^{ON}$ | $N_2^{ON}$ | $N_3^{ON}$ | $N_4^{ON}$ | $P_{1GS}^{SH}$ | $P_{1GD}^{SH}$ | $P_{1DS}^{SH}$ | $P_{2GS}^{SH}$ | $P_{2GD}^{SH}$ | $P_{2DS}^{SH}$ | $N_{1GS}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | 1 a | 1 a | 1 n | 1 a | 1 a | 1 n | 1 n |
| 0 1 | 1 n | 1 n | 1 n | 1 a | 1 n | 1 a | 1 n | 1 n | 1 n | 1 n | 0 a | 0 a | 1 n | 1 n |
| 1 0 | 1 n | 1 n | 1 n | 1 n | $I^*$ a | 1 n | 1 a | 0 a | 0 a | 1 n | 1 n | 1 n | 1 n | 1 n |
| 1 1 | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | 0 n | 0 n | $I^*$ a | 1 a | 0 n | 1 a | 1 a | 1 a |
| *Input* | $N_{1GD}^{SH}$ | $N_{1DS}^{SH}$ | $N_{2GS}^{SH}$ | $N_{2GD}^{SH}$ | $N_{2DS}^{SH}$ | $N_{3GS}^{SH}$ | $N_{3GD}^{SH}$ | $N_{3DS}^{SH}$ | $N_{4GS}^{SH}$ | $N_{4GD}^{SH}$ | $N_{4DS}^{SH}$ | $Q_{1ce}^{SH}$ | $Q_{1bc}^{SH}$ | $Q_{1be}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 a | 1 n | 1 n | 1 n | 1 n | 1 n | 1 a | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | $D_{0-1}$ n |
| 0 1 | 0 a | 1 a | 1 a | 1 a | 1 n | 1 n | 1 a | 1 a | 1 a | 1 a | 1 n | 1 n | 1 n | $D_{0-1}$ n |
| 1 0 | 1 n | 1 n | 1 n | $I^*$ a | 0 a | 1 n | 1 n | 1 n | 1 n | 1 a | 1 a | 1 n | 1 n | $D_{0-1}$ n |
| 1 1 | 1 a | 0 n | 1 a | 1 a | 0 n | 1 a | 1 a | 0 n | 1 a | 1 a | 0 n | 1 a | 1 a | 0 n |

X = Output, i = Current drawn by the device, $Q^n$ = Previous State,

$ON$ = Stuck-ON, $SH$ = Short, (G, S, D = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts), (e, b, c = emitter, base, collector),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-3 A,

$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,

fault-free behavior for all input vectors except for input vector '10' which causes the previous state to be retained resulting in sequential behavior. Similar sequential behavior is observed for $P_2$ stuck-open with input vector '01'. Two pattern tests can be applied to detect these stuck-open failures. Summary of the behavior of S-BJT BiCMOS NAND with Stuck-OPEN faults for all transistors is given in Table 2.

s-OPEN failures of transistors $N_1$ and $N_2$ exhibit unique delay faults. A first glance would lead one to expect that with input vectors 11, the output parasitic capacitance would be discharged by turning ON of transistors $N_3$ and $N_4$. However, due to the open fault of transistor $N_1$ or $N_2$ under consideration, the vectors 00, 01 or 10 would charge up the parasitic capacitors at the base as well as the emitter nodes of the bipolar transistors. With the application of input vector 11, the series path of $N_3$ and $N_4$ will be turned ON but the series path of $N_1$ and $N_2$ will not be turned on due to the fault. This will cause transistor $Q_1$ to remain ON for sometime because of the charge stored at the base of the bipolar transistor. Transistor $Q_1$ would be discharged slowly through the ON resistance of $N_3$ and $N_4$ alone causing delay in the output response. The slow to fall delay fault is shown in Figure 9a,b & c. This type of fault has been observed in [9] for a different implementation of a BiCMOS NAND.

Figures 9a & b show the response of the BiCMOS NAND to $N_1^{OP}$ failure with one CMOS load and with RC load respectively. Figure 9a shows the response of BiCMOS NAND to $N_1^{OP}$ with only one CMOS load connected to the BiCMOS output. The inputs shown in this figure are the inputs applied to the BiCMOS NAND and the input pulse width ($t_{pw}$) is 10ns wide. The response of the BiCMOS NAND with $N_1^{OP}$ fault with input $t_{pw}$=10ns shows slow to fall delay ($t_{hl2}$) of 7.2ns instead of the normal propagation delay ($t_{hl1}$) of 0.6ns. Response of BiCMOS output with RC load shown in Figure 9b causes High to Low transition delay for both fault-free and $N_1^{OP}$ response, due to higher fan-out. Here, the output level barely reaches the logic '0' level. It should be noticed that if the clock period is small, the voltage at the output will be in the indeterminate range or will not drop below valid '1' range. The response of the BiCMOS NAND with $N_1^{OP}$ fault with $t_{pw}$=10ns and with RC load shows slow to fall delay ($t_{hl2}$) of 7.9ns instead of the normal propagation delay ($t_{hl1}$) of 1.835ns. Figure 9c shows the response with input $t_{pw}$=4ns, where the faulty output does not have time enough to go below logic '1' range. The response of the fault-free BiCMOS NAND with input $t_{pw}$=4ns gives a propagation delay of 1.835ns.

For the s-OPEN failures of transistors $N_3$ and $N_4$ with input vector 11, there is no conduction path for the charge stored in the output parasitic capacitances to be discharged. With the input vector of 11, transistors $N_1$ and $N_2$ turn ON and results in a voltage close to 0V at the base of the bipolar transistor. If the input vector applied prior to the input vector 11 was

Table 2: Behavior of S-BJT BiCMOS NAND with Stuck-OPEN faults for all transistors.

| **Single BJT BiCMOS NAND results** | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $P_1^{OP}$ | $P_2^{OP}$ | $N_1^{OP}$ | $N_2^{OP}$ | $N_3^{OP}$ | $N_4^{OP}$ | | | |
| $Input$ | $ff$ | $P_{1SGD}^{OP}$ | $P_{2SGD}^{OP}$ | $N_{1SGD}^{OP}$ | $N_{2SGD}^{OP}$ | $N_{3SGD}^{OP}$ | $N_{4SGD}^{OP}$ | $Q_{1e}^{OP}$ | $Q_{1b}^{OP}$ | $Q_{1c}^{OP}$ |
| A B | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | R | R | $D_{0-1}$ |
| 0 1 | 1 | 1 | $Q^n$ | 1 | 1 | 1 | 1 | R | R | $D_{0-1}$ |
| 1 0 | 1 | $Q^n$ | 1 | 1 | 1 | 1 | 1 | R | R | $D_{0-1}$ |
| 1 1 | 0 | 0 | 0 | $D_{1-0}$ | $D_{1-0}$ | S | S | 0 | 0 | 0 |

X = Output, $Q^n$ = Previous State, (e, b, c = emitter, base, collector), $OP$ = Open,
$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts), ($G$, $S$, $D$ = Gate, Source, Drain),
$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,
R = Stuck-at-0 after initialization, S = Stuck-at-1 after initialization.

00, 01 or 10, it would charge the output to a logic '1' level. This would effectively appear as input stuck-at-1 after initialization, which is a special case of sequential behavior ($Q^n$).

Bipolar transistor emitter and base s-OPEN faults manifest as stuck-at-0 after initialization (shown as R in Table 2). It can be seen that with either of the above faults, output cannot go to logic '1' (other than during power up) as no path exists between output and $V_{DD}$. With collector open, the output exhibits Low to High transition delay ($D_{0-1}$) as shown in Figures 10a,b & c. Figure 10a shows the response of BiCMOS NAND to $Q_1$ collector open with one CMOS load connected to the BiCMOS output. The inputs shown in this figure are the inputs applied to BiCMOS NAND. The response of the BiCMOS NAND with $Q_1$ collector open for $t_{pw}$=10ns shows Low to High transition delay ($t_{lh2}$) of 0.579ns instead of the normal Low to High transition delay ($t_{lh1}$) of 0.289ns. Response of BiCMOS NAND with RC load shown in Figure 10b exhibits Low to High transition delay ($t_{lh2}$) of 1.449ns instead of the normal Low to High transition delay ($t_{lh1}$) of 0.483ns. Figure 10c shows the response with input $t_{pw}$ = 4ns, where the faulty output exhibits larger delay for the low to high transition. The faulty low to high transition delay was seen to be $t_{hl2}$ = 1.449ns instead of the normal low to high transition delay of $t_{hl1}$ = 0.483ns.

Figure 10: (a) BiCMOS response to $Q_{1C}^{OPEN}$ with $t_{pw}$=10ns & One CMOS Load (b) $t_{pw}$=10ns & RC Load (c) $t_{pw}$=4ns & RC Load.

# 5 Analysis of Physical Failures in D-BJT BiCMOS devices

In this section, the response of the D-BJT BiCMOS NAND shown in Figure 5 is evaluated for hard failures of the bipolar & MOS transistors and the results are given in Tables 3 and 4.

## 5.1 Stuck-ON faults in D-BJT BiCMOS NAND

Stuck-ON faults in S-BJT BiCMOS NAND generally result in a fault-free logic level, faulty logic level or indeterminate logic level. However, in all the cases, it results in enhanced $I_{DDQ}$

Referring to the D-BJT BiCMOS NAND shown in Figure 5, for the physical failure $P_1^{ON}$, the device behaves similar to fault-free gate for all input vectors except for input vector '11'. Input vector '11' causes the N-devices ($N_1$, $N_2$, $N_3$ and $N_4$) to be ON. This causes transistor $Q_2$ to be ON, providing a conduction path from $V_{DD}$ to $V_{SS}$(Gnd), resulting in enhanced $I_{DDQ}$. The current drawn by the device with this vector for the fault under consideration is $\approx$2mA instead of the normal $\approx$0.2$\mu$A. Current testing technique can be employed to detect this fault. Similar result is observed for transistor $P_2$ stuck-ON failure ($P_2^{ON}$). SPICE simulation indicates the output voltage level to be $\approx$1.63V, which is logic '0' level for BiCMOS devices indicated as '0' in Table 3.

Transistor $N_1$ stuck-ON fault results in an enhanced $I_{DDQ}$ for input vector '01'. Similarly, enhanced $I_{DDQ}$ is observed for transistor $N_2$ stuck-ON fault with input vector '10'. SPICE simulation indicates the output voltage to be 1.86V, which is logic '0' level for D-BJT BiCMOS devices.

Stuck-ON failures of transistors $N_3$ and $N_4$ result in enhanced $I_{DDQ}$ for input vectors 01 and 10 respectively. The fault-free and faulty logic levels for $N_3$ and $N_4$ stuck-ON failures exhibit logic '1' at the output. Since the fault-free and faulty logic levels are the same, current testing alone can detect the failures.

Transistor $N_5$ stuck-ON failure does not cause any appreciable effect for output Low to High transitions. However, during output High to Low transitions, with input vector '11', the output finds a low resistance path through transistors $N_3$, $N_4$ and $N_5$. Due to this low resistance path, transistor $Q_2$ does not turn ON and hence, High to Low transition gets delayed. This delay is dependent upon the output load. For RC load, the High to Low transition delay was observed to be 1.45ns instead of the normal 0.89ns. It may be noted that due to the low resistance path through transistors $N_3$, $N_4$ and $N_5$, output goes all the way to ground instead of $Gnd$+$V_{BE(Q2)}$.

Transistor $Q_{1ce}^{SH}$ and $Q_{1bc}^{SH}$ shorts result in enhanced $I_{DDQ}$ and causes a faulty output logic

Table 3: Behavior of D-BJT BiCMOS NAND with Stuck-ON and short between terminals for all transistors.

| **Double BJT BiCMOS NAND with Stuck-ON and Short results** | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | *ff* | $P_1^{ON}$ | $P_2^{ON}$ | $N_1^{ON}$ | $N_2^{ON}$ | $N_3^{ON}$ | $N_4^{ON}$ | $N_5^{ON}$ | $P_{1GS}^{SH}$ | $P_{1GD}^{SH}$ | $P_{1DS}^{SH}$ | $P_{2GS}^{SH}$ | $P_{2GD}^{SH}$ | $P_{2DS}^{SH}$ | $N_{1GS}^{SH}$ | $N_{1GD}^{SH}$ | $N_{1DS}^{SH}$ | $N_{2GS}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | 1 a | 1 a | 1 n | 1 a | 1 a | 1 n | 1 n | 1 a | 1 n | 1 n |
| 0 1 | 1 n | 1 n | 1 n | 0 a | 1 n | 1 a | 1 n | 1 n | 1 n | 1 n | 1 n | 0 a | 0 a | 1 n | 1 n | 0 a | 0 a | 1 a |
| 1 0 | 1 n | 1 n | 1 n | 1 n | 0 a | 1 n | 1 a | 1 n | 0 a | 0 a | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n | 1 n |
| 1 1 | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | 0 n | $D_{1-0}$ n | 0 n | $I^*$ a | 1 a | 0 n | $I^*$ a | 1 a | 1 a | $I^*$ a | 0 n | 1 a |
| *Input* | *ff* | $N_{2GD}^{SH}$ | $N_{2DS}^{SH}$ | $N_{3GS}^{SH}$ | $N_{3GD}^{SH}$ | $N_{3DS}^{SH}$ | $N_{4GS}^{SH}$ | $N_{4GD}^{SH}$ | $N_{4DS}^{SH}$ | $N_{5GS}^{SH}$ | $N_{5GD}^{SH}$ | $N_{5DS}^{SH}$ | $Q_{1ce}^{SH}$ | $Q_{1bc}^{SH}$ | $Q_{1be}^{SH}$ | $Q_{2ce}^{SH}$ | $Q_{2bc}^{SH}$ | $Q_{2be}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 1 n | 1 n | 1 n | 1 a | 1 n | 1 n | 1 n | 1 n | 0 a | 0 a | 1 n | 1 n | 1 n | $D_{0-1}$ n | 0 a | 0 a | 1 n |
| 0 1 | 1 n | 1 a | 1 n | 1 n | $I^*$ a | $I^*$ a | 1 a | 1 a | 1 n | 0 a | 0 a | 1 n | 1 n | 1 n | $D_{0-1}$ n | 0 a | 0 a | 1 n |
| 1 0 | 1 n | 0 a | 0 a | 1 n | 1 n | 1 n | 1 n | 1 a | 1 a | 0 a | 0 a | 1 n | 1 n | 1 n | $D_{0-1}$ n | 0 a | 0 a | 1 n |
| 1 1 | 0 n | $I^*$ a | 0 n | 1 a | $I^*$ a | 0 n | 1 a | $I^*$ a | 0 n | 0 n | 0 n | $D_{1-0}$ n | 1 a | 1 a | 0 n | 0 n | 0 n | $D_{1-0}$ n |

X = Output, i = Current drawn by the device, $Q^n$ = Previous State,

$ON$ = Stuck-ON, $SH$ = Short, (G, S, D = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (2.2-2.7Volts), (e, b, c = emitter, base, collector),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-3 A,

$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,

level '1' for input vector 11. Transistor $Q_{2ce}^{SH}$ and $Q_{2bc}^{SH}$ also result in enhanced $I_{DDQ}$ and causes a faulty output logic level '0' for input vectors 00, 01 and 10. Transistor $Q_{1be}^{SH}$ and $Q_{2be}^{SH}$ result in delay faults for Low to High transition and High to Low transitions respectively, as the base to emitter junction of the transistors do not get forward biased and hence do not get turned ON. The Low to High transition delay observed for $Q_{1be}^{SH}$ with RC output load is 1.98ns compared to the fault-free delay of 1.07ns. The High to Low transition delay observed for $Q_{2be}^{SH}$ with RC output load is 1.47ns compared to the fault-free delay of 0.89ns.

Current testing can be very effective for testing failures which result in elevated $I_{DDQ}$ from a normal $\approx 0.2\mu$A to enhanced $\approx$2mA, an increase by a factor of $\approx 10^4$. Since stuck-ON failures $P_1^{ON}$, $P_2^{ON}$, $N_3^{ON}$ and $N_4^{ON}$ provide same logic level for faulty as well as fault-free operations, current testing alone can detect the failures. Transistor $N_1$ and $N_2$ stuck-ON as well as $Q_{1ce}^{SH}$, $Q_{1bc}^{SH}$,$Q_{2ce}^{SH}$, and $Q_{2bc}^{SH}$ failures exhibit dissimilar outputs under faulty and fault-free conditions, conventional logic testing can detect the failure. However, current testing would detect this failure mode. Transistor $Q_1$ & $Q_2$ base to emitter shorts manifest as Low to High and High to Low transition delays respectively and hence delay test alone would detect the failure modes.

Table 4: Behavior of D-BJT BiCMOS NAND with Stuck-OPEN faults for all transistors.

| **Single BJT BiCMOS NAND results** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $Input$ | $ff$ | $P_1^{OP}$ $P_{1SGD}^{OP}$ | $P_2^{OP}$ $P_{2SGD}^{OP}$ | $N_1^{OP}$ $N_{1SGD}^{OP}$ | $N_2^{OP}$ $N_{2SGD}^{OP}$ | $N_3^{OP}$ $N_{3SGD}^{OP}$ | $N_4^{OP}$ $N_{4SGD}^{OP}$ | $N_5^{OP}$ $N_{5SGD}^{OP}$ | $Q_{1e}^{OP}$ | $Q_{1b}^{OP}$ | $Q_{1c}^{OP}$ | $Q_{2e}^{OP}$ | $Q_{2b}^{OP}$ | $Q_{2e}^{OP}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $D_{0-1}$ | R | R | $D_{0-1}$ | 1 | 1 | 1 |
| 0 1 | 1 | 1 | $Q^n$ | 1 | 1 | 1 | 1 | $D_{0-1}$ | R | R | $D_{0-1}$ | 1 | 1 | 1 |
| 1 0 | 1 | $Q^n$ | 1 | 1 | 1 | 1 | 1 | $D_{0-1}$ | R | R | $D_{0-1}$ | 1 | 1 | 1 |
| 1 1 | 0 | 0 | 0 | $D_{1-0}$ | $D_{1-0}$ | $D_{1-0}$ | $D_{1-0}$ | 0 | 0 | 0 | 0 | $D_{1-0}$ | $D_{1-0}$ | $D_{1-0}$ |

X = Output, $Q^n$ = Previous State, (e, b, c = emitter, base, collector), $OP$ = Open,
$ff$ = fault free, $I^*$ = Indeterminate (2.2-2.7Volts), ($G$, $S$, $D$ = Gate, Source, Drain),
$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,
R = Stuck-at-0 after initialization, S = Stuck-at-1 after initialization.

## 5.2 Stuck-OPEN faults in D-BJT BiCMOS NAND

Stuck-OPEN faults in D-BJT BiCMOS NAND result in either sequential behavior or delay faults.

Two faults in the D-BJT BiCMOS NAND exhibit sequential behavior ($Q_n$), similar to the behavior seen in CMOS circuits. Presence of the fault $P_1$ stuck-OPEN would result in fault-free behavior for all input vectors except for input vector '10' which causes the previous state to be retained resulting in sequential behavior. Similar sequential behavior is observed for $P_2$ stuck-open with input vector '01'. Two pattern tests can be applied to detect these stuck-open failures. Summary of the behavior of D-BJT BiCMOS NAND with Stuck-OPEN faults for all transistors is given in Table 4.

S-OPEN failures of transistors $N_1$ and $N_2$ exhibit unique delay faults, as observed in S-BJT BiCMOS NAND. A first glance would lead one to expect that with input vectors '11', the output parasitic capacitance would be discharged by turning ON of transistors $N_3$, $N_4$ and $Q_2$. However, due to the OPEN fault of $N_1$ or $N_2$ under consideration, the vectors 00, 01 or 10 would charge up the parasitic capacitors at the base as well as the emitter nodes of the bipolar transistor $Q_1$. With the application of input vector 11, the series path of $N_3$ and $N_4$ will be turned ON but the series path of $N_1$ and $N_2$ will not be turned ON due to the fault. This will cause transistor $Q_1$ to remain ON for sometime because of the charge stored at the base of the bipolar transistor $Q_1$. Transistor $Q_1$ would be discharged slowly through $N_3$, $N_4$ and $Q_2$ path alone causing delay in the output response. The slow to fall delay fault is shown in Figure 11a,b&c. This type of fault has been observed in [9]. Figures 11a&b show the response

of the D-BJT BiCMOS NAND to $N_1^{OP}$ failure with one CMOS output load and input pulse width $t_{pw}$ of 10ns and 4ns respectively. Figure 11a shows the response of the BiCMOS NAND to $N_1^{OP}$ with only one CMOS connected to the BiCMOS output. The inputs shown in this figure are the inputs applied to the BiCMOS NAND and the input pulse width ($t_{pw}$) is 10ns wide. The response of the BiCMOS NAND with $N_1^{OP}$ fault with input $t_{pw}$=10ns shows slow to fall delay ($t_{hl2}$) of 4.5ns instead of the normal propagation delay ($t_{hl1}$) of 0.526ns. Response of the BiCMOS output with the same one CMOS load and with $t_{pw}$ of 4ns causes a High to Low delay of 7.2ns instead of the normal propagation delay of 0.58ns. As the clock period is small, it should be noticed here that the output barely reaches the switching threshold and the logic level does not have a chance to drop to logic '0' range. If the clock period is further reduced or if the output load is increased, the output level will not have a chance to reach even the switching threshold. An example of which is shown in Figure 11c where an RC load is used in addition to a CMOS load. It can be seen that the output does not have a chance to reach the switching threshold. The response of the fault-free BiCMOS NAND with $t_{pw}$=4ns and RC load gives a propagation delay of 0.79ns.

Response of stuck-OPEN failure of $N_4$ are shown in Figures 12a,b&c. For the stuck-OPEN failure of $N_4$ shown in Figure 12a, with input vector '11' exhibits a delay ($t_{hl2}$) of 1.204ns and output logic level of 1V instead of the normal propagation delay of 0.526ns and logic level of 0.6V, with one CMOS load and input pulse width $t_{pw}$ of 10ns. Reducing the pulse width $t_{pw}$ to 4ns exhibits a delay ($t_{hl2}$) of 1.25ns in place of the normal $t_{hl1}$ of 0.58ns as shown in Figure 12b. The output level is observed to be $\approx$1.5V instead of the normal output level of $\approx$0.6V, however, the output logic level is still a valid logic '0' level of D-BJT BiCMOS devices. With RC load and input pulse width $t_{pw}$ of 4ns, the output logic level does not fall below the logic threshold as shown in Figure 12c. Hence, the fault appears as stuck-at-1 for logic testing purposes.

Bipolar transistor $Q_1$ emitter and base open faults manifest as stuck-at-0 after initialization (shown as R in Table 4). It can be seen that with either of the above faults, output cannot go to logic '1' (other than during power up) as no path exists between output and $V_{DD}$. With Bipolar transistor $Q_1$ collector open, the output exhibits Low to High transition delay ($D_{0-1}$) as shown in Figures 13a,b&c. Figure 13a shows the response of BiCMOS NAND to $Q_1$ collector open with one CMOS load connected to the BiCMOS output and with input pulse width $t_{pw}$ of 10ns shows Low to High transition ($t_{lh2}$) delay of 1.08ns instead of the normal Low to High transistion ($t_{hl1}$) of 0.823ns. Response with the same one CMOS load and with input pulse width ($t_{pw}$) of 4ns exhibits Low to High transition delay ($t_{lh2}$) of 1.105ns instead of the normal propagation delay ($t_{lh1}$) of 0.72ns as shown in Figure 13b. Figure 13c shows the response of the BiCMOS NAND with input $t_{pw}$=4ns and RC load where the faulty output

exhibits a larger delay for the Low to High transition. The faulty Low to High transition delay is seen to be $t_{lh2}$=2.3ns instead of the normal Low to High transition delay of $t_{lh1}$=0.91ns.

Bipolar transistor $Q_2$ emitter, base & collector open faults manifest as High to Low delay faults. Response of D-BJT BiCMOS NAND base and emitter opens are shown in Figures 13a,b&c. With one CMOS load and input $t_{pw}$ of 10ns shows a delay ($t_{hl2}$) of 1.059ns instead of the normal propagation delay ($t_{hl1}$) of 0.526ns for $Q_2$ base open. However, $Q_2$ emitter exhibits a lower delay compared to $Q_2$ base open. With input $t_{pw}$ of 4ns and with one CMOS load, the output exhibits a delay ($t_{hl2}$) of 1.68ns instead of the normal propagation delay ($t_{hl1}$) of 0.58ns. With RC load at the output of the BiCMOS NAND input $t_{pw}$ of 4ns, the output exhibits a delay ($t_{hl2}$) of 3.22ns instead of the normal propagation delay ($t_{hl1}$) of 0.79ns, for transistor $Q_2$ base open. Transistor $Q_2$ emitter open with input $t_{pw}$ of 4ns exhibits stuck-at-1 behavior since before the input can make a transition to output low, the input undergoes transition to opposite logic level. If the input pulse width ($t_{pw}$) is made wider, the output would go to the other side of the logic threshold.

Transistor $N_5$ serves the purpose of discharging the base of $Q_2$ quickly to speed up the output Low to High transition [20]. Stuck-OPEN failure of transistor $N_5$ can be expected to result in delayed Low to High transition.

There is an interesting observation during output High to Low transition which needs mentioning. During output High to Low transition and with $N_5$ stuck-OPEN, it is observed that the output transition speeds up and causes enhanced dynamic current ($I_{DD}$) as shown in Figure 14. This can be explained as follows. Under normal operation with $N_5$ fault-free, any of the input vectors 00,01 or 10 causing output high(1), turns ON transistor $N_5$, thereby base of $Q_2$ remains discharged, keeping transistor $Q_2$ OFF. With transistor $N_5$ stuck-OPEN, any of the input vectors 00, 01 or 10 causing output high(1), will not be able to turn ON transistor $N_5$ and discharge base of $Q_2$. This causes some base bias to exist at the base of transistor $Q_2$. The base bias existing at the base of $Q_2$ may be sufficient enough to turn ON the device partially. Since the input vectors 00, 01 or 10 are intended to turn ON transistor $Q_1$ to provide output High, with $Q_2$ also partially ON, enhanced dynamic $I_{DD}$ is observed. It may be noted that given sufficient time the current may decay to Zero. Hence, this probably cannot be termed as enhanced $I_{DDQ}$ fault and so this is being termed as enhanced dynamic $I_{DD}$ fault. $I_{DDQ}$ testing may detect this fault as the enhanced dynamic $I_{DD}$ current is about 2 orders of magnitude greater than fault-free current, just after the initial transient. Due to the existence of residual base bias on transistor $Q_2$, with input vector 11, turns transistor $Q_2$ ON faster than fault-free where no residual base bias exists. Hence, the speed up for output High to Low transition. The fault-free output High to Low transition delay is observed to be 0.90ns and with transistor $N_5$ stuck-OPEN 0.43ns, resulting in 0.47ns early transition than

that of fault-free.

Figure 12: (a) BiCMOS response to $N_4^{OPEN}$ with $t_{pw}$=10ns & One CMOS Load (b) $t_{pw}$=4ns & One CMOS Load (c) $t_{pw}$=4ns & RC Load.

Figure 14: BiCMOS response to $N_5^{OPEN}$ and Fault-free with RC Load (a) Voltage levels at BiCMOS output and $Q_2$ base (b) Plot illustrating enhanced dynamic $I_{DD}$.

Figure 15: An S-BJT BiCMOS NOR.

# 6 Physical Failures in BiCMOS NOR, CMOS and TTL Devices

In this section, the response of Single and Double BJT BiCMOS NOR, CMOS NAND and NOR as well as TTL NAND and NOR are evaluated for hard failures of the MOS and Bipolar transistors.

## 6.1 Physical Failures in BiCMOS NOR

In this subsection, the response of the Single and Double BJT BiCMOS NOR gates are evaluated for hard failures of the MOS and Bipolar transistors.

Possible failures considered are stuck-ON and stuck-OPEN of transistors. The output of the BiCMOS NOR gate is obtained by simulating one failure at a time for all possible stuck-ON and stuck-OPEN failures for all transistors. Stuck-ON and stuck-OPEN were simulated by turning ON and turning OFF the respective transistors. Open (OP) in transistor terminals were simulated by connecting a resistance of R>1M$\Omega$ in series with the respective node and short (SH) were simulated by connecting a hard short of R<0.01$\Omega$ between the respective terminals.

The response of S-BJT BiCMOS NOR shown in Figure 15 for stuck-ON in transistors and shorts (SH) between terminals is given in Table 5

The response of S-BJT BiCMOS NOR shown in Figure 15 for stuck-OPEN in transistors and between terminals is given in Table 6

The response of D-BJT BiCMOS NOR shown in Figure 16 for stuck-ON in transistors and shorts (SH) between terminals is given in Table 7

Table 5: Behavior of S-BJT BiCMOS NOR with Stuck-ON and Short faults between terminals for all transistors.

| **Single BJT BiCMOS NOR Stuck-ON and Short results** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | *ff* | $P_1^{ON}$ | $P_2^{ON}$ | $N_1^{ON}$ | $N_2^{ON}$ | $N_3^{ON}$ | $N_4^{ON}$ | $P_{1GS}^{SH}$ | $P_{1GD}^{SH}$ | $P_{1DS}^{SH}$ | $P_{2GS}^{SH}$ | $P_{2GD}^{SH}$ | $P_{2DS}^{SH}$ | $N_{1GS}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 1 n | 1 n | 0 a | 0 a | 1 a | 1 a | 0 a | 0 a | 1 n | 0 a | 0 a | 1 n | 1 n |
| 0 1 | 0 n | 0 n | 0 a | 0 n | 0 n | 0 n | 0 n | 0 a | 0 a | 0 n | 0 n | 0 a | 0 a | 0 n |
| 1 0 | 0 n | 0 a | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | 1 a |
| 1 1 | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 a |
| *Input* | $N_{1GD}^{SH}$ | $N_{1DS}^{SH}$ | $N_{2GS}^{SH}$ | $N_{2GD}^{SH}$ | $N_{2DS}^{SH}$ | $N_{3GS}^{SH}$ | $N_{3GD}^{SH}$ | $N_{3DS}^{SH}$ | $N_{4GS}^{SH}$ | $N_{4GD}^{SH}$ | $N_{4DS}^{SH}$ | $Q_{1ce}^{SH}$ | $Q_{1bc}^{SH}$ | $Q_{1be}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 0 a | 0 a | 1 n | 0 a | 0 a | 0 a | 0 a | 0 a | 1 n | 0 a | 0 a | 1 n | 1 n | $D_{0-1}$ n |
| 0 1 | 0 n | 0 n | 1 a | 0 a | 0 n | 0 n | 0 n | 0 n | 1 a | 1 a | 0 n | 1 a | 1 a | 0 n |
| 1 0 | 0 a | 0 n | 0 n | 0 n | 0 n | 0 a | 1 a | 0 n | 0 n | 0 n | 0 n | 1 a | 1 a | 0 n |
| 1 1 | 0 a | 0 n | 0 n | 0 a | 0 n | 0 a | 0 a | 0 n | 0 a | 0 a | 0 n | 1 a | 1 a | 0 n |

X = Output, i = Current drawn by the device, $Q^n$ = Previous State,

$ON$ = Stuck-ON, $OP$ = Stuck-Open, $SH$ = Short, (G, S, D = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts), (e, b, c = emitter, base, collector),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-2 A,

$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,

Table 6: Behavior of S-BJT BiCMOS NOR with Stuck-OPEN faults for all transistors.

| **Single BJT BiCMOS NOR results** | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | *ff* | $P_1^{OP}$ $P_{1SGD}^{OP}$ | $P_2^{OP}$ $P_{2SGD}^{OP}$ | $N_1^{OP}$ $N_{1SGD}^{OP}$ | $N_2^{OP}$ $N_{2SGD}^{OP}$ | $N_3^{OP}$ $N_{3SGD}^{OP}$ | $N_4^{OP}$ $N_{4SGD}^{OP}$ | $Q_{1e}^{OP}$ | $Q_{1b}^{OP}$ | $Q_{1c}^{OP}$ |
| A B | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | $Q^n$ | $Q^n$ | 1 | 1 | 1 | 1 | R | R | $D_{0-1}$ |
| 0 1 | 0 | $Q^n$ | $Q^n$ | 0 | $D_{1-0}$ | 0 | $Q^n$ | R | R | 0 |
| 1 0 | 0 | $Q^n$ | $Q^n$ | $D_{1-0}$ | 0 | $Q^n$ | 0 | R | R | 0 |
| 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

X = Output, $Q^n$ = Previous State, (e, b, c = emitter, base, collector)

$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts), ($G$, $S$, $D$ = Gate, Source, Drain),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-2 A,

$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,

R = Stuck-at-0 after initialization.

Figure 16: An D-BJT BiCMOS NOR.

Table 7: Behavior of D-BJT BiCMOS NOR with Stuck-ON and short between terminals for all transistors.

| **Double BJT BiCMOS NOR with Stuck-ON and Short results** | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | *ff* | $P_1^{ON}$ | $P_2^{ON}$ | $N_1^{ON}$ | $N_2^{ON}$ | $N_3^{ON}$ | $N_4^{ON}$ | $N_5^{ON}$ | $P_{1GS}^{SH}$ | $P_{1GD}^{SH}$ | $P_{1DS}^{SH}$ | $P_{2GS}^{SH}$ | $P_{2GD}^{SH}$ | $P_{2DS}^{SH}$ | $N_{1GS}^{SH}$ | $N_{1GD}^{SH}$ | $N_{1DS}^{SH}$ | $N_{2GS}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 1 n | 1 n | 0 a | 0 a | $I^*$ a | $I^*$ a | 1 n | 0 a | 0 a | 1 n | 0 a | 0 a | 1 n | 1 n | 0 a | 0 a | 1 n |
| 0 1 | 0 n | 0 n | 0 a | 0 n | 0 n | 0 n | 0 n | $D_{1-0}$ n | 0 a | 0 a | 0 n | 0 n | $I^*$ a | 0 a | 0 n | 0 n | 0 n | 1 a |
| 1 0 | 0 n | 0 a | 0 n | 0 n | 0 a | 0 n | 0 n | $D_{1-0}$ n | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | 1 a | $I^*$ a | 0 n | 0 n |
| 1 1 | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | $D_{1-0}$ n | 0 n | 0 n | 0 n | 0 n | 0 a | 0 n | 0 a | 0 a | 0 n | 0 a |
| *Input* | *ff* | $N_{2GD}^{SH}$ | $N_{2DS}^{SH}$ | $N_{3GS}^{SH}$ | $N_{3GD}^{SH}$ | $N_{3DS}^{SH}$ | $N_{4GS}^{SH}$ | $N_{4GD}^{SH}$ | $N_{4DS}^{SH}$ | $N_{5GS}^{SH}$ | $N_{5GD}^{SH}$ | $N_{5DS}^{SH}$ | $Q_{1ce}^{SH}$ | $Q_{1bc}^{SH}$ | $Q_{1be}^{SH}$ | $Q_{2ce}^{SH}$ | $Q_{2bc}^{SH}$ | $Q_{2be}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 0 n | 0 a | 1 n | $I^*$ a | 0 a | 1 n | $I^*$ a | 0 a | 0 a | 0 a | 1 n | 1 n | 1 n | $D_{0-1}$ n | 0 a | 0 a | 1 n |
| 0 1 | 0 n | $I^*$ a | 0 n | 0 a | 0 n | 0 n | 1 a | $I^*$ a | 0 n | 0 n | 0 n | $D_{1-0}$ n | 1 a | 1 a | 0 n | 0 n | 0 n | $D_{1-0}$ n |
| 1 0 | 0 n | 0 n | 0 n | 0 a | $I^*$ a | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | $D_{1-0}$ n | 1 a | 1 a | 0 n | 0 n | 0 n | $D_{1-0}$ n |
| 1 1 | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | $D_{1-0}$ n | 1 a | 1 a | 0 n | 0 n | 0 n | $D_{1-0}$ n |

X = Output, i = Current drawn by the device, $Q^n$ = Previous State,

$ON$ = Stuck-ON, $OP$ = Stuck-Open, $SH$ = Short, (G, S, D = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (2.2-2.7Volts), (e, b, c = emitter, base, collector),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-2 A,

$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,

Table 8: Behavior of D-BJT BiCMOS NOR with Stuck-OPEN faults for all transistors.

| Double BJT BiCMOS NOR results | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $P_1^{OP}$ | $P_2^{OP}$ | $N_1^{OP}$ | $N_2^{OP}$ | $N_3^{OP}$ | $N_4^{OP}$ | $N_5^{OP}$ | | | | | | |
| $Input$ | $ff$ | $P_{1SGD}^{OP}$ | $P_{2SGD}^{OP}$ | $N_{1SGD}^{OP}$ | $N_{2SGD}^{OP}$ | $N_{3SGD}^{OP}$ | $N_{4SGD}^{OP}$ | $N_{5SGD}^{OP}$ | $Q_{1e}^{OP}$ | $Q_{1b}^{OP}$ | $Q_{1c}^{OP}$ | $Q_{2e}^{OP}$ | $Q_{2b}^{OP}$ | $Q_{2c}^{OP}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | $Q^n$ | $Q^n$ | 1 | 1 | 1 | 1 | $D_{0-1}$ | R | R | $D_{0-1}$ | 1 | 1 | 1 |
| 0 1 | 0 | $Q^n$ | $Q^n$ | 0 | $D_{1-0}$ | 0 | $Q^n$ | 0 | 0 | 0 | 0 | $D_{1-0}$ | $D_{1-0}$ | $D_{1-0}$ |
| 1 0 | 0 | $Q^n$ | $Q^n$ | $D_{1-0}$ | 1 | $Q^n$ | 0 | 0 | 0 | 0 | 0 | $D_{1-0}$ | $D_{1-0}$ | $D_{1-0}$ |
| 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $D_{1-0}$ | $D_{1-0}$ | $D_{1-0}$ |

X = Output, $Q^n$ = Previous State,

$ff$ = fault free, $I^*$ = Indeterminate (2.2-2.7Volts), ($G$, $S$, $D$ = Gate, Source, Drain),

$D_{0-1}$= Low to High transition delay, $D_{1-0}$ = High to Low transition delay,

R = Stuck-at-0 after initialization.

The response of D-BJT BiCMOS NOR shown in Figure 16 for stuck-OPEN in transistors and between terminals is given in Table 8

## 6.2 Physical Failures in CMOS NAND and NOR

In this subsection, the response of the CMOS NAND and NOR gates are evaluated for hard failures of the MOS transistors.

Possible failures considered are stuck-ON and stuck-OPEN of transistors. The output of the CMOS gate is obtained by simulating one failure at a time for all possible stuck-ON and stuck-OPEN failures for all transistors. Stuck-ON and stuck-OPEN were simulated by turning ON and turning OFF the respective transistors. Open (OP) in transistor terminals (source, gate & drain) were simulated by connecting a resistance of R>1MΩ in series with the respective node and short (SH) were simulated by connecting a hard short of R<0.01Ω between the respective terminals.

The response of CMOS NAND shown in Figure 17 for stuck-ON in transistors and shorts (SH) between terminals is given in Table 9.

The response of CMOS NAND shown in Figure 17 for stuck-OPEN in transistors and between terminals is given in Table 10.

The response of CMOS NOR shown in Figure 18 for stuck-ON in transistors and shorts (SH) between terminals is given in Table 11.

The response of CMOS NOR shown in Figure 18 for stuck-OPEN in transistors and between terminals is given in Table 12.

Figure 17: A CMOS NAND Gate.

Table 9: Behavior of CMOS NAND with Stuck-ON and Short faults between terminals for all transistors.

| **Results for CMOS NAND Stuck-ON and Short between terminals** | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | $ff$ | $P_1^{ON}$ | $P_2^{ON}$ | $N_1^{ON}$ | $N_2^{ON}$ | $P_{1GS}^{SH}$ | $P_{1GD}^{SH}$ | $P_{1DS}^{SH}$ | $P_{2GS}^{SH}$ | $P_{2GD}^{SH}$ | $P_{2DS}^{SH}$ | $N_{1GS}^{SH}$ | $N_{1GD}^{SH}$ | $N_{1DS}^{SH}$ | $N_{2GS}^{SH}$ | $N_{2GD}^{SH}$ | $N_{2DS}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 1 n | 1 n | 1 n | 1 n | 1 a | 1 a | 1 n | 1 a | 1 a | 1 n | 1 n | 1 a | 1 n | 1 n | 1 n | 1 n |
| 0 1 | 1 n | 1 n | 1 n | 0 a | 1 n | 0 a | 0 a | 1 n | 1 n | 1 n | 1 n | 1 n | 0 a | 0 a | 1 a | 1 a | 1 n |
| l 1 0 | 1 n | 1 n | 1 n | 1 n | 0 a | 1 n | 1 n | 1 n | 0 a | 0 a | 1 n | 1 n | 1 n | 1 n | 1 n | 0 a | 0 a |
| 1 1 | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | 1 a | 1 a | 0 n | 1 a | 1 a | 1 a | 1 a | 0 n | 1 a | 1 a | 0 n |

X = Output, $Q^n$ = Previous State, ($G$, $S$, $D$ = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-2 A,

Table 10: Behavior of CMOS NAND with Stuck-OPEN faults for all transistors.

| **CMOS NAND Open results** | | | | | |
|---|---|---|---|---|---|
| | | $P_1^{OP}$ | $P_2^{OP}$ | $N_1^{OP}$ | $N_2^{OP}$ |
| *Input* | $ff$ | $P_{1SGD}^{OP}$ | $P_{2SGD}^{OP}$ | $N_{1SGD}^{OP}$ | $N_{2SGD}^{OP}$ |
| A B | X | X | X | X | X |
| 0 0 | 1 | 1 | 1 | 1 | 1 |
| 0 1 | 1 | $Q^n$ | 1 | 1 | 1 |
| 1 0 | 1 | 1 | $Q^n$ | 1 | 1 |
| 1 1 | 0 | 0 | 0 | 1 | 1 |

X = Output, $Q^n$ = Previous State, ($G$, $S$, $D$ = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-2 A,

Table 11: Behavior of CMOS NOR with Stuck-ON and Short faults between terminals for all transistors.

| **Results for CMOS NOR Stuck-ON and Short between terminals** | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $Input$ | $ff$ | $P_1^{ON}$ | $P_2^{ON}$ | $N_1^{ON}$ | $N_2^{ON}$ | $P_{1GS}^{SH}$ | $P_{1GD}^{SH}$ | $P_{1DS}^{SH}$ | $P_{2GS}^{SH}$ | $P_{2GD}^{SH}$ | $P_{2DS}^{SH}$ | $N_{1GS}^{SH}$ | $N_{1GD}^{SH}$ | $N_{1DS}^{SH}$ | $N_{2GS}^{SH}$ | $N_{2GD}^{SH}$ | $N_{2DS}^{SH}$ |
| A B | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i | X i |
| 0 0 | 1 n | 1 n | 1 n | 0 a | 0 a | 0 a | 0 a | 1 n | 0 a | 0 a | 1 n | 1 n | 0 a | 0 a | 1 n | 0 a | 0 a |
| 0 1 | 0 n | 0 n | 0 a | 0 n | 0 n | 0 a | 0 a | 0 n | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | 1 a | 0 a | 0 n |
| 1 0 | 0 n | 0 a | 0 n | 0 n | 0 n | 0 n | 0 a | 0 a | 0 n | 0 n | 0 n | 1 a | $I^*$ a | 0 n | 0 n | 0 n | 0 n |
| 1 1 | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 n | 0 a | 0 n | 0 a | 0 a | 0 n | 0 a | 0 a | 0 n |

X = Output, $Q^n$ = Previous State, ($G$, $S$, $D$ = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-2 A,

Table 12: Behavior of CMOS NOR with Stuck-OPEN faults for all transistors.

| **CMOS NOR Open results** | | | | | |
|---|---|---|---|---|---|
| | | $P_1^{OP}$ | $P_2^{OP}$ | $N_1^{OP}$ | $N_2^{OP}$ |
| $Input$ | $ff$ | $P_{1SGD}^{OP}$ | $P_{2SGD}^{OP}$ | $N_{1SGD}^{OP}$ | $N_{2SGD}^{OP}$ |
| A B | X | X | X | X | X |
| 0 0 | 1 | 0 | 0 | 1 | 1 |
| 0 1 | 0 | 0 | 0 | 0 | $Q^n$ |
| 1 0 | 0 | 0 | 0 | $Q^n$ | 0 |
| 1 1 | 0 | 0 | 0 | 0 | 0 |

X = Output, $Q^n$ = Previous State, ($G$, $S$, $D$ = Gate, Source, Drain),

$ff$ = fault free, $I^*$ = Indeterminate (1.5-2.0Volts),

n (Normal Current) = 2e-7 A, a (Abnormal Current) > 2.00e-2 A,

Figure 18: A CMOS NOR Gate.

## 6.3 Physical Failures in TTL NAND and NOR

In this subsection, the response of the TTL NAND and NOR gates are evaluated for hard failures of the bipolar transistors.

Possible failures considered are SHORTS and OPENS in transistors. The output of the TTL gate is obtained by simulating one failure at a time for all possible OPEN and SHORT failures for all transistors. Open (OP) in transistor terminals (emitter, base & collector) were simulated by connecting a resistance of R>1MΩ in series with the respective node and short (SH) were simulated by connecting a hard short of R<0.01Ω between the respective terminals.

The response of TTL NAND shown in Figure 19 for shorts (SH) between terminals of transistors is given in Table 13.

The response of TTL NAND shown in Figure 19 for OPEN between terminals of transistors is given in Table 14.

The response of TTL NOR shown in Figure 20 for shorts (SH) between terminals of transistors is given in Table 15.

The response of TTL NOR shown in Figure 20 for OPEN between terminals of transistors is given in Table 16.

# 7 Comparison of the three logic families (TTL, CMOS, BiCMOS)

Summary of faulty behavior of single and double BJT BiCMOS, CMOS and TTL NAND and NOR devices are given in Tables 17 & 18 respectively. While analysis of single and double BJT BiCMOS NAND devices are presented in sections 4 and 5, analysis of BiCMOS as well as

Figure 19: A TTL NAND Gate.

Table 13: Behavior of TTL NAND with short between terminals for all transistors.

| **TTL NAND Short results** | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | $ff$ | $Q^{SH}_{1be}$ | $Q^{SH}_{1bc}$ | $Q^{SH}_{1ce}$ | $Q^{SH}_{2be}$ | $Q^{SH}_{2ce}$ | $Q^{SH}_{3be}$ | $Q^{SH}_{3bc}$ | $Q^{SH}_{3ce}$ | $Q^{SH}_{4be}$ | $Q^{SH}_{4bc}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | $I^*$ | 0 | 0 | 0 | $I^*$ |
| *Input* | $Q^{SH}_{4ce}$ | $Q^{SH}_{5be}$ | $Q^{SH}_{5bc}$ | $Q^{SH}_{5ce}$ | $D^{SH}_{1}$ | $D^{SH}_{2}$ | $D^{SH}_{3}$ | $R^{SH}_{1}$ | $R^{SH}_{2}$ | $R^{SH}_{3}$ | $R^{SH}_{4}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 1 | $I^*$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | $I^*$ | 0 | 1 |

X = Output, $SH$ = Short, (e, b, c = Emitter, Base, Collector),

$ff$ = fault free, $I^*$ = Indeterminate (0.8-2.4Volts),

Figure 20: A TTL NOR Gate.

Table 15: Behavior of TTL NOR with short between terminals for all transistors.

| **TTL NOR Short results** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | *ff* | $Q_{1be}^{SH}$ | $Q_{1bc}^{SH}$ | $Q_{1ce}^{SH}$ | $Q_{2be}^{SH}$ | $Q_{2bc}^{SH}$ | $Q_{2ce}^{SH}$ | $Q_{3be}^{SH}$ | $Q_{3bc}^{SH}$ | $Q_{3ce}^{SH}$ | $Q_{4be}^{SH}$ | $Q_{4bc}^{SH}$ | $Q_{4ce}^{SH}$ | $Q_{5be}^{SH}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | $I^*$ | 0 | 0 | 0 | 0 | $I^*$ | 0 |
| 1 0 | 0 | 0 | 0 | $I^*$ | $I^*$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 1 | 0 | 0 | 0 | $I^*$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $I^*$ | 0 |
| *Input* | *ff* | $Q_{5bc}^{SH}$ | $Q_{5ce}^{SH}$ | $Q_{6be}^{SH}$ | $Q_{6bc}^{SH}$ | $Q_{6ce}^{SH}$ | $D_1^{SH}$ | $D_2^{SH}$ | $D_3^{SH}$ | $R_1^{SH}$ | $R_2^{SH}$ | $R_3^{SH}$ | $R_4^{SH}$ | $R_5^{SH}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 1 | 1 | 1 | $I^*$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 1 | 0 | 0 | $I^*$ | 1 | $I^*$ | 0 | 0 | 0 | 0 | 0 | $I^*$ | 0 | 0 | 1 |
| 1 0 | 0 | 0 | $I^*$ | 1 | $I^*$ | 0 | 0 | 0 | 0 | 0 | $I^*$ | 0 | 0 | 1 |
| 1 1 | 0 | 0 | $I^*$ | 1 | $I^*$ | 0 | 0 | 0 | 0 | 0 | $I^*$ | 0 | 0 | 1 |

X = Output, $SH$ = Short, (e, b, c = Emitter, Base, Collector),

$ff$ = fault free, $I^*$ = Indeterminate (0.8-2.4Volts),

Table 16: Behavior of TTL NOR with open between terminals for all transistors.

| **TTL NOR Open results** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *Input* | *ff* | $Q_{1e}^{OP}$ | $Q_{1b}^{OP}$ | $Q_{1c}^{OP}$ | $Q_{2e}^{OP}$ | $Q_{2b}^{OP}$ | $Q_{2c}^{OP}$ | $Q_{3e}^{OP}$ | $Q_{3b}^{OP}$ | $Q_{3c}^{OP}$ | $Q_{4e}^{OP}$ | $Q_{4b}^{OP}$ | $Q_{4c}^{OP}$ | $Q_{5e}^{OP}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| l 1 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| *Input* | *ff* | $Q_{5b}^{OP}$ | $Q_{5c}^{OP}$ | $Q_{6e}^{OP}$ | $Q_{6b}^{OP}$ | $Q_{6c}^{OP}$ | $D_1^{OP}$ | $D_2^{OP}$ | $D_3^{OP}$ | $R_1^{OP}$ | $R_2^{OP}$ | $R_3^{OP}$ | $R_4^{OP}$ | $R_5^{OP}$ |
| A B | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| 0 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

X = Output, $SH$ = Short, (e, b, c = Emitter, Base, Collector),

$ff$ = fault free, $I^*$ = Indeterminate (0.8-2.4Volts),

Table 17: Summary of faulty behavior in BiCMOS, CMOS and Bipolar(TTL) NAND Gates.

| **Summary of BiCMOS, CMOS & TTL NAND gates** | | | | |
|---|---|---|---|---|
| Type of faulty Behavior | BiCMOS NAND (S-BJT) | BiCMOS NAND (D-BJT) | CMOS NAND | TTL NAND |
| **Fault-free** | — | — | — | **12(29.27%)** |
| **Indeterminate Output** | **—** | **—** | **—** | **4(9.76%)** |
| **Logic Testable Faults:** | **18(33.33%)** | **10(14.66%)** | **16(50%)** | **25(60.97%)** |
| Stuck-at-0 or 1 | 10(18.52%) | 2(2.9%) | 8(25%) | 25(60.97%) |
| Sequential Behavior | 8(14.81%) | 8(11.76%) | 8(25%) | — |
| **Delay Testable Faults:** | **10(18.52%)** | **28(41.18%)** | **—** | **—** |
| **Current Testable Faults:** | **26(48.15%)** | **30(44.12%)** | **16(50%)** | |
| Logic Testable | 17(31.48%) | 22(32.35%) | 14(43.75%) | — |
| Not Logic Testable | 9(16.67%) | 8(11.77%) | 2(6.25%) | **—** |

CMOS and TTL NAND & NOR are given in Section 6. Response of the respective devices is evaluated for hard failures of the components (MOS & bipolar transistors and resistors). All possible failures such as, stuck-ON and stuck-OPEN of transistors, opens and shorts between terminals are considered.

From Tables 17 & 18, the conclusions that can be drawn are given below. While faults in TTL devices manifest either as logic testable or indeterminate output, CMOS devices exhibit either as logic testable or current testable faults. 25% of the faults in CMOS devices manifest as stuck-at and 25% as sequential behavior. Out of the 50% of the faults in CMOS NAND and NOR which manifest as current testable faults, 43.75% in CMOS NAND and 34.38% in CMOS NOR are logic testable. However, 6% and 16% of the current testable faults in CMOS NAND and NOR devices are not logic testable, which means that only $I_{DDQ}$ testing would detect the faults in a definite way. About 26% of the faults in single and double BJT NAND as well as NOR devices manifest as current testable faults, out of which almost 11 to 17% of the faults are not logic testable and hence, for these faults, only $I_{DDQ}$ monitoring would ensure detection. For D-BJT BiCMOS devices, transistor $N_5$ open fault manifesting as enhanced dynamic $I_{DD}$ current is not included as current testable fault in Tables 17 & 18. However, the enhanced dynamic $I_{DD}$ current can be detected using $I_{DDQ}$ monitoring techniques. 18.5% of the faults in S-BJT NAND & NOR and 28% & 20% of the faults in D-BJT NAND and NOR are delay fault testable.

From the above summary on the behavior of S-BJT and D-BJT BiCMOS devices vis-a-vis CMOS and TTL devices, it can be seen that a major portion of the faults in S-BJT and

Table 18: Summary of faulty behavior in BiCMOS, CMOS and Bipolar(TTL) NOR Gates.

| **Summary of BiCMOS, CMOS & TTL NOR gates** | | | | |
|---|---|---|---|---|
| Type of faulty Behavior | BiCMOS NOR (S-BJT) | BiCMOS NOR (D-BJT) | CMOS NOR | TTL NOR |
| **Fault-free** | — | — | — | **14(26.92%)** |
| **Indeterminate Output** | — | — | — | **7(13.46%)** |
| **Logic Testable Faults:** | **18(33.33%)** | **18(26.47%)** | **16(50%)** | **31(59.62%)** |
| Stuck-at-0 or 1 | 2(3.7%) | 2(2.94%) | 8(25%) | 31(59.62%) |
| Sequential Behavior | 16(29.63%) | 16(23.53%) | 8(25%) | — |
| **Delay Fault** | **10(18.52%)** | **20(29.41%)** | — | — |
| **Current Testable Faults:** | **26(48.15%)** | **30(44.12%)** | **16(50%)** | — |
| Logic Testable | 20(37.04%) | 20(32.35%) | 11(34.38%) | — |
| Not Logic Testable | 6(11.11%) | 10(14.71%) | 5(15.62%) | — |

D-BJT devices manifest either as current testable fault or as delay testable fault. This makes $I_{DDQ}$ testing as well as delay testing methodologies important for BiCMOS devices. Current monitoring techniques [23, 24, 10] can be used to detect such faults. A scheme for current monitoring ($I_{DDQ}$) for BiCMOS devices is presented in [25]. In addition to current testable faults, BiCMOS devices exhibit delay testable faults too. Hence, the strategy for BiCMOS devices are much more complicated than CMOS and TTL devices. Testability and testing issues in BiCMOS are addressed in the next section.

# 8 Testability of BiCMOS Devices

In S-BJT and D-BJT BiCMOS devices, apart from sequential behavior, current testable as well as delay testable faults are present.

Stuck-ON faults in BiCMOS devices result in either same logic level as fault-free or different logic level from that of fault-free. In all cases, enhanced $I_{DDQ}$ results due to a direct path from $V_{DD}$ to $V_{SS}$(Gnd). Hence, current testing ($I_{DDQ}$ monitoring) techniques can be implemented to detect such failures. When the logic level under faulty conditions are different from that of fault-free, logic monitoring as well as current testing will detect the fault. However, when the logic level under faulty conditions is the same as fault-free, current testing alone can detect the fault.

Stuck-OPEN faults in BiCMOS devices can exhibit sequential behavior or delay fault [9, 10, 11, 25]. Detection of such sequential behavior due to s-OPEN faults in CMOS requires two

Figure 21: Proposed testable design for testable BiCMOS gate using (a) pMOS DFT transistors, (b) nMOS DFT transistors

pattern tests instead of a single pattern [6, 26, 27, 28]. The first pattern is applied to initialize the output of the gate and the second pattern to detect the fault [29, 30]. For detection of an s-OPEN fault in the p-part(n-part), the first pattern sets the output to logic ZERO (logic ONE). The second pattern then attempts to provide a low-resistance path between the output and the power-supply (ground) through the faulty transistor. To avoid invalidation of tests in the presence of timing skews, robust two-pattern tests have been suggested. In such robust sequences, the Hamming distance between the initialization pattern and the second test pattern is kept at unity [31, 32, 33], so as to avoid the possible intermediate state.

Stuck-OPEN failures in n-part(1) in both S-BJT and D-BJT NAND devices manifest as delay faults. Test generation for detection of delay faults are more difficult. One method of detecting faults manifesting as sequential behavior is by applying two pattern tests or multi-pattern sequences. A Design for Testability (DFT) technique [36] has been developed for detection of such faults in S-BJT circuits. The DFT scheme developed uses only 2 additional transistors and only a single vector instead of the two or multi-pattern sequences to detect stuck-OPEN failures in the presence of timing skews/delays, glitches or charge sharing among internal nodes. The Design for Testability scheme [34, 35, 36] developed avoids the requirement of generating tests for detection of delay faults.

The testable design scheme allows testing the n-parts and the combination of p-part & bipolar separately, thus facilitating the use of a single test vector to detect a s-OPEN fault. Instead of forcing the output to a high-impedance state to test for s-OPEN sequential behavior or delay fault, the output node is connected to the power supply(ground) during the testing of n-parts (p-part & bipolar) through a resistance that is significantly higher than the ON resistances of the n- or p-parts.

Since the n-parts and the combination of p-part & bipolar are complementary to each other, when a vector turns the n-part ON, the combination of p-part & bipolar are turned OFF and vice-versa. The proposed testable design uses two transistors (DFT or Design for Testability transistors), either two pMOS transistors or two nMOS transistors can be used as shown in Figures 21(a),(b). One of the transistors is connected to the CMOS output of the BiCMOS device (base of bipolar transistor) and the other to the output of the BiCMOS device (emitter of the bipolar transistor). The switching of these pass transistors are controlled by an external signal $C_p$ and the value passed is provided externally by the signal $C_t$. Two external control signals ($C_p$ & $C_t$) and two p- or n-transistors are used in the proposed design as shown in Figures 21(a) & (b).

The extra transistors provide a static load at the output. The dimensions of the extra transistors should be chosen such that the ON resistance of the transistors are considerably higher than the ON resistances of the p-part as well as the n-parts. With the use of pMOS

Table 19: Summary of input vectors needed under normal and test conditions.

| **Summary** | | |
|---|---|---|
| Mode | pMOS DFT Transistors | nMOS DFT Transistors |
| | $C_p$ $C_t$ | $C_p$ $C_t$ |
| Normal Operation | 1 X | 0 X |
| Testing n-parts | 0 1 | 1 1 |
| Testing p-part | 0 0 | 1 0 |

transistor, for example, when $C_p$=0, the gate is essentially transformed to a pseudo nMOS gate [22]. Therefore, the standard rules in designing pseudo nMOS (pseudo pMOS) type structures can be used to determine the size of the extra transistors. In general, a minimum size transistor, which offers a resistance of about 5-6 times that of the ON resistance of the p- or n-parts are sufficient to provide the correct voltage levels.

Table 19 summarizes the input vectors needed under normal and test modes with pMOS/nMOS transistors as DFT transistors. The test vector for detection of stuck-open fault in either of the n-parts is $C_pC_t$=11(01) with nMOS(pMOS) DFT transistors, and a Zero Vertex (0Vx) covering the interested nMOS transistor. Zero Vertex 0Vx(One Vertex 1Vx) is an input vector to a logic gate, which produces an output logic value Zero(One) in the fault-free gate. The 0Vx will turn the p-part and the Bipolar OFF. Therefore, both parts of the augmented gate will appear as pull down n-part(1) & (2) and pull-up $T_{n1}$,$T_{n2}$($T_{p1}$,$T_{p2}$). If s-OPEN fault is present in n-part(2), it will cause a high-resistance path between the output and ground resulting in logic ONE(1) at the output. If an s-OPEN fault is present in n-part(1), it will cause a high-resistance path between the base of the bipolar transistor and ground. With the application of 0Vx and with the DFT transistors nMOS(pMOS) turned ON, the base of the bipolar transistor would be ≈5V due to the s-OPEN fault in n-part(1) which turns the bipolar transistor ON. 0Vx turns the n-part(2) ON but due to the wired-OR property [10] exhibited by the S-BJT device, resulting output is logic ONE(1). Hence, the output will appear to be logic ONE(1) for both n-part(1) as well as n-part(2) s-OPEN failures. If the fault is not present, 0Vx will provide a low resistance path from bipolar transistor base to ground and output to ground. As the ON resistance of $T_{p1}$,$T_{p2}$($T_{n1}$,$T_{n2}$) is considerably higher than the ON resistance of the n-part, the output will appear as logic ZERO(0). Therefore, a single test vector will detect the fault.

Similarly, consider an s-OPEN fault in the p-part. The test vector for this fault is $C_p$ $C_t$ = 10(00) with nMOS(pMOS) DFT transistors, and a ONE Vertex (1Vx), covering the interested

pMOS transistor. The 1Vx will turn the n-parts(1) & (2) OFF causing pull up p-part, bipolar transistor and pull down $T_{n1}$,$T_{n2}$($T_{p1}$,$T_{p2}$). If an s-OPEN fault is present in the p-part, it will cause a high resistance path between the base of the bipolar transistor and $V_{DD}$. With the application of 1Vx and with the DFT transistors nMOS(pMOS) turned ON, the base and emitter nodes of the bipolar transistor would be ≈0V leading to logic '0' at the output. If the base, emitter or collector nodes of the bipolar transistor is open, with the application of 1Vx and with the DFT transistors nMOS(pMOS) turned ON, the output results in logic '0'. If the fault is not present 1Vx will provide low resistance path from bipolar transistor base and out put to $V_{DD}$. As the ON resistance of $T_{p1}$,$T_{p2}$($T_{n1}$,$T_{n2}$) is considerably higher than the ON resistance of the p-part, the output will appear as logic ONE(1). Therefore, a single test vector will detect the fault.

# 9 Conclusions

Physical failures causing transistor stuck-OPEN in Single BJT and Double BJT BiCMOS devices were examined. In addition to sequential behavior observed in CMOS devices, BiCMOS devices also exhibit delay faults. Some of the stuck-ON faults can be detected by observing voltage level, however, power supply current ($I_{DDQ}$) monitoring would definitely detect the fault. A stuck-OPEN faults in double BJT BiCMOS device exhibiting enhanced dynamic $I_{DD}$ current was presented. Faulty behavior of the three different families, namely, TTL, CMOS and BiCMOS were compared to bring out the testability differences between the three logic families. Since many stuck-OPEN faults manifest as delay faults, this failure needs to be considered as an important criteria for testing/test generation of BiCMOS devices. Testability of both Single BJT and Double BJT BiCMOS devices were discussed.

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